

**ADDvantage-32**  
**AC TO DC POWER CONVERTER**  
**(Includes AFM - Advanced Firing Module)**  
**For Use With Software Part Numbers**  
**692xxx and 694xxx**

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## **PROPRIETARY NOTE**

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## **WARRANTY**

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# ADDvantage-32 AC TO DC POWER CONVERTER

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## **SAFETY SUMMARY**

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### **W A R N I N G**

**HAZARDOUS VOLTAGES ARE USED IN THE OPERATION OF THIS EQUIPMENT AND MAY CAUSE SEVERE PERSONAL INJURY OR THE LOSS OF LIFE IF PROPER PRECAUTIONS ARE NOT TAKEN. THE FOLLOWING PRECAUTIONS SHOULD BE TAKEN TO REDUCE THE RISK OF INJURY OR DEATH.**

\*\*\*\*\*

### **W A R N I N G**

**SEPARATE MOTOR OVERCURRENT, OVERLOAD, AND OVERHEATING PROTECTION IS REQUIRED TO BE PROVIDED IN ACCORDANCE WITH THE CANADIAN ELECTRICAL CODE, PART I.**

\*\*\*\*\*

### **A V E R T I S S E M E N T**

**LE MOTEUR DOIT ETRE MUNI D'UNE PROTECTION DISTINCTE CONTRE LES SURINTENSITES, LA SURCHARGE ET LA SURCHAUFFE CONFORMEMENT AU CODE CANADIAN DE L'ELECTRICITE, PREMIERE PARTIE.**

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### **D A N G E R**

**HAZARDOUS VOLTAGE WILL CAUSE SEVERE INJURY AND DEATH. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE SERVICING.**

\*\*\*\*\*

### **D A N G E R**

**PRESENCE DE TENSIONS DANGEREUSES POUVANT ET PERTE DE VIE. COUPER L'ALIMENTATION AVANT LE DEPANNAGE DE CET EQUIPMENT.**

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### **W A R N I N G**

DO NOT OPERATE RADIO TRANSMITTERS or CELL PHONES IN THE VICINITY OF THE ADD-32. The ADD-32 is an electronic device. Although it is designed to operate reliably in typical industrial environments, the ADD-32 can be affected by radio and/or cell phone transmitters. It is possible to cause drive faults, inappropriate/unintended drive I/O activity, and unpredictable operation that could result in damage to the ADD-32, damage to other equipment, or serious injury to personnel.

Radio transmitter interference is a site specific phenomena. Generally, electrical wires connected to terminals on the ADD-32 are the conduits for radio interference. Interference can be minimized by good wiring design and installation practice. It is recommended that signs be posted in and around the drive system, warning of the possibility of interference if the drive is in operation. DO NOT USE radio transmitters or cell phones in the area.

Absence of a radio interference problem is no guarantee that a problem will never occur as conditions and environments can change.

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## WARNING

### System Safety Considerations ADD-32 DOK Fault Contact

The ADD-32 is a sophisticated microprocessor device incorporating many self diagnostic tests. The function of its DOK (Drive OK) fault contact is to detect a variety of faults in the ADD-32, but it cannot assure fault-free operation.

BE AWARE THAT NOT ALL ADD-32 FAULTS CAN BE SELF DIAGNOSED AND/OR ALARMED. THEREFORE, THE ADD-32 CANNOT BE CONSIDERED TO BE FAIL SAFE NOR CAN ITS "DOK" CONTACT BE RELIED ON TO RESPOND TO ALL POSSIBLE ADD-32 FAULT CONDITIONS.

The "DOK" contact should be incorporated into system interlock logic chains to ensure safe system response to a drive fault "DOK" output contact opening. It is the responsibility of the system designer to understand the system interlock logic chains and to apply the "DOK" contact appropriately.

IN SAFETY SENSITIVE APPLICATIONS, IT IS STRONGLY SUGGESTED THAT THE SYSTEM DESIGNER UTILIZE A SEPARATE MONITORING DEVICE TO CHECK THE ADD-32 INPUTS AND OUTPUTS, AND OTHER OPERATING CHARACTERISTICS, TO ENHANCE THE SAFETY OF PERSONNEL AND PROPERTY.

\*\*\*\*\*

1. Only qualified personnel familiar with this equipment should be permitted to install, operate, troubleshoot, or repair the apparatus after reading and understanding this manual.
2. Installation of the equipment must be performed in accordance with the National Electrical Code and any other state or local codes. Proper grounding, conductor sizing, and short circuit protection must be installed for safe operation.
3. During normal operation, keep all covers in place and cabinet doors shut.
4. When performing hands-on inspections and maintenance, be sure the incoming AC feed is turned off and locked out. The ADD-32 and motor may have hazardous voltages present

4. When performing hands-on inspections and maintenance, be sure the incoming AC feed is turned off and locked out. The ADD-32 and motor may have hazardous voltages present even if the AC feed is turned off. **\*\*NOTE\*\* THE ARMATURE CONTACTOR DOES NOT REMOVE HAZARDOUS VOLTAGES WHEN OPENED.**
5. When necessary to take measurements with the power turned on, do not touch any electrical connection points. Remove all jewelry from wrists and fingers. Make sure test equipment is in safe operating condition.
6. While servicing with the power on, stand on approved insulating material and be sure not to be grounded.
7. Follow the instructions in this manual carefully and observe all danger notices.

\*\*\*\*\*

### W A R N I N G

**ACCURACY OF CUSTOMER-INSTALLED CALIBRATION AND CONFIGURATION DATA IS IMPERATIVE IN THE OPERATION OF THIS EQUIPMENT. INCORRECT DATA MAY CAUSE DAMAGE TO THE ADD-32, MOTOR, AND PROCESS EQUIPMENT.**

\*\*\*\*\*

8. The National Electric Code requires that the end-use customer field mark all electrical control panels and distribution equipment with an accurate: Arc Flash Hazard Boundary, an Arc Flash Hazard Category, and the level of the required Personal Protective Equipment (PPE).

The marking shall be per the requirements of the most current version of NFPA 70 (National Electric Code). The specific marking requirements can be found in the most current version of NFPA 70 E (Standard for Electrical Safety Requirement for the Employee Work Place).



ADDvantage-32  
AC TO DC POWER CONVERTER  
(Includes AFM - Advanced Firing Module)

**SECTION I**  
**INTRODUCTION AND**  
**GENERAL INFORMATION**

**1.1 DESCRIPTION**

The ADDvantage-32™ Digital AC to DC Power Converter (ADD-32) provides variable coordinated control, process communication, and on-line status information. It provides digital control to DC motors with armature voltages up to 500 VDC and permanent magnet or shunt wound fields up to 300 VDC.

This manual includes information about the Avtron Advanced Firing Module (AFM), which is used in retrofit applications that retain existing SCR power conversion. The AFM incorporates all the control and diagnostic functions of the ADDvantage-32™ up to and including pulse transformers to fire the existing SCRs.

**STANDARD FEATURES INCLUDE:**

- Advanced 32-bit, 20 MHz RISC microprocessor
- Fully digital controlled SCR armature bridge and field power converter
- Maintenance keypad with a 2-line alphanumeric digital display of plain English messages and engineering units
- 12 status LED indicators (one user definable)
- Integral 4-Channel, high speed memory signal analyzer
- Fully digital, standard control loops which may include:
  - armature current regulation
  - field current regulation
  - speed control regulation
  - tension control regulation
  - center driven winder regulation

- Tach loss and overspeed protection, configurable with automatic switchover to a redundant digital tach or armature voltage feedback.
- Heat sink overtemperature warning
- DC motor temperature sensing with overtemperature protection
- AC line fuses and a DC link fuse on regenerative units  
(DC link fuse is only used on units rated 10 through 510 and 550 ADC)
- Individual semiconductor fuses in each leg of SCR bridge (applies to units rated at 850A and above)
- Fully rated DC contactor with optional DB pole available
- Chassis type construction
- Instantaneous Over Current (IOC) protection
- Phase loss/Phase sequence protection
- Field current loss protection
- Field economy
- Low AC line voltage and frequency protection
- 16 event Fault FIFO
- All drive information accessible by remote operator interface over a RS485 multidrop link or 802.4 LAN
- Retentive setpoints (not available in 690XXX software)

## **1.2      HARDWARE AND EQUIPMENT FEATURES**

Figures 1-1, 1-2, and 1-3 illustrate the three typical hardware configurations of the ADDvantage-32 Power Converters. Each hardware configuration contains a microprocessor board, system board, bridge interface board, and a power base. Hardware configuration varies with the output rating of the ADDvantage-32 being used.

Figure 1-4 shows a typical Advanced Firing Module. The AFM hardware generally includes the same items listed above except for the power base.



10 through 510 (Figure 1-1) and 550 ADC (Figure 1-2) Power Converters

ADDvantage-32's rated for 10 through 510 and 550 ADC are packaged as a single unit. "Brick style" or rectangular SCR's are mounted in the power base and allow for convenient packaging.

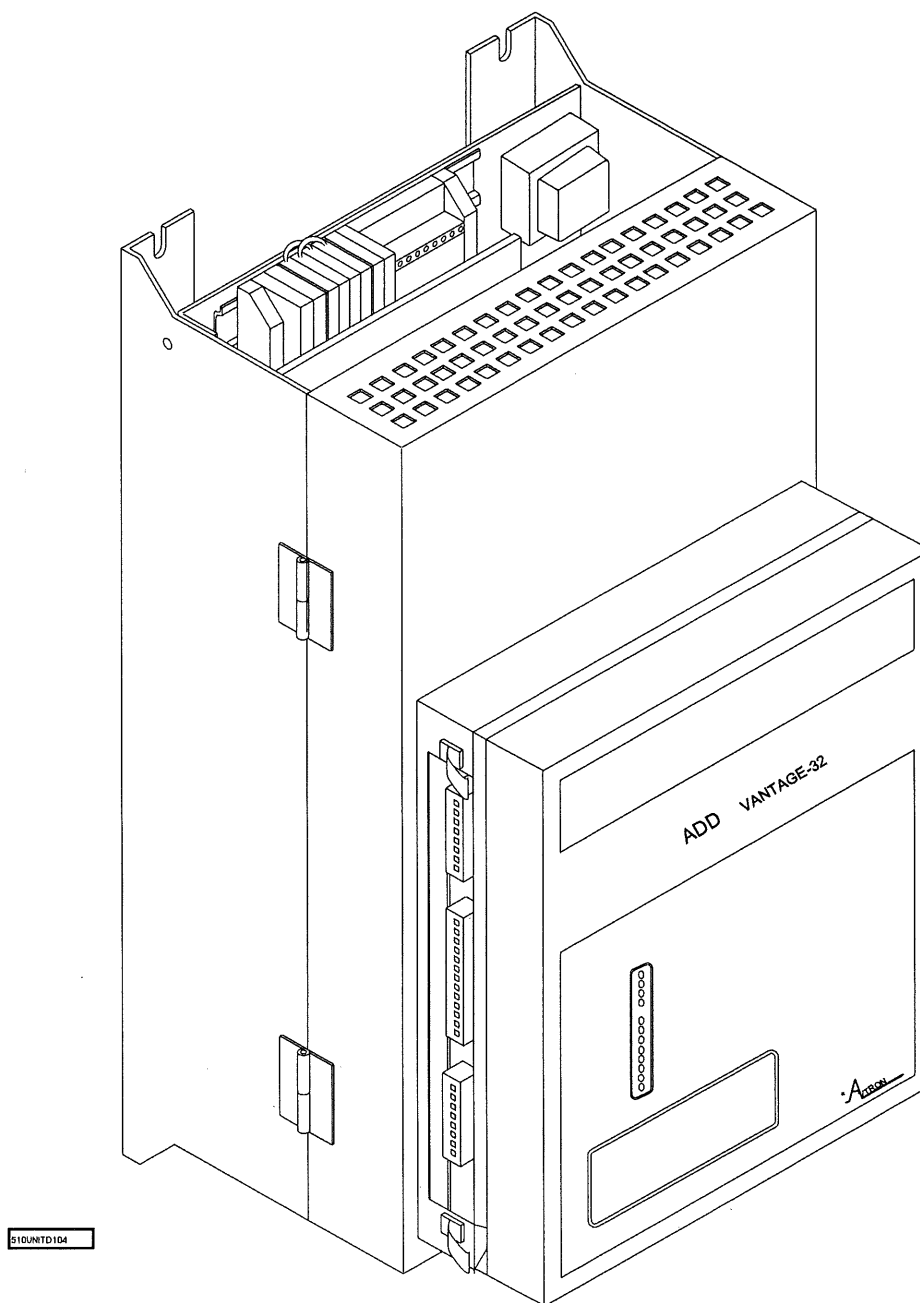


Figure 1-1. ADDvantage-32 AC to DC Power Converter  
(510 ADC and Below)

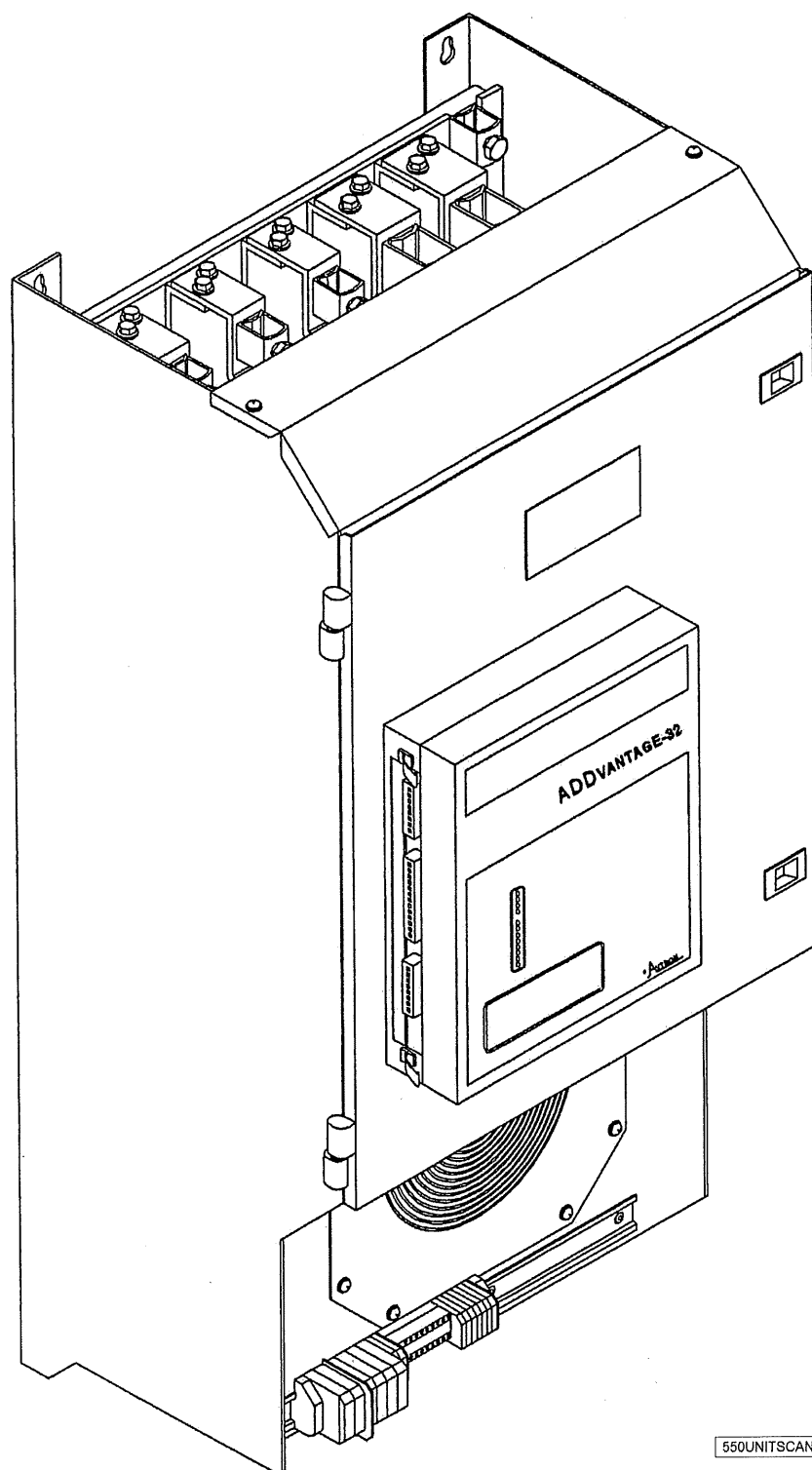


Figure 1-2. ADDvantage-32™ AC to DC Power Converter (550 ADC)

540, 850, 1550, and 3000 ADC Power Converters

Units rated at 540, 850, 1550, and 3000 ADC consist of two modules. The microprocessor, system, and bridge interface boards are mounted inside the Controller and Field Supply Assembly to allow for easier installation. "Hockey Puck" style or circular SCR's are mounted to individual heat sinks which are housed in the Armature Bridge Assembly.

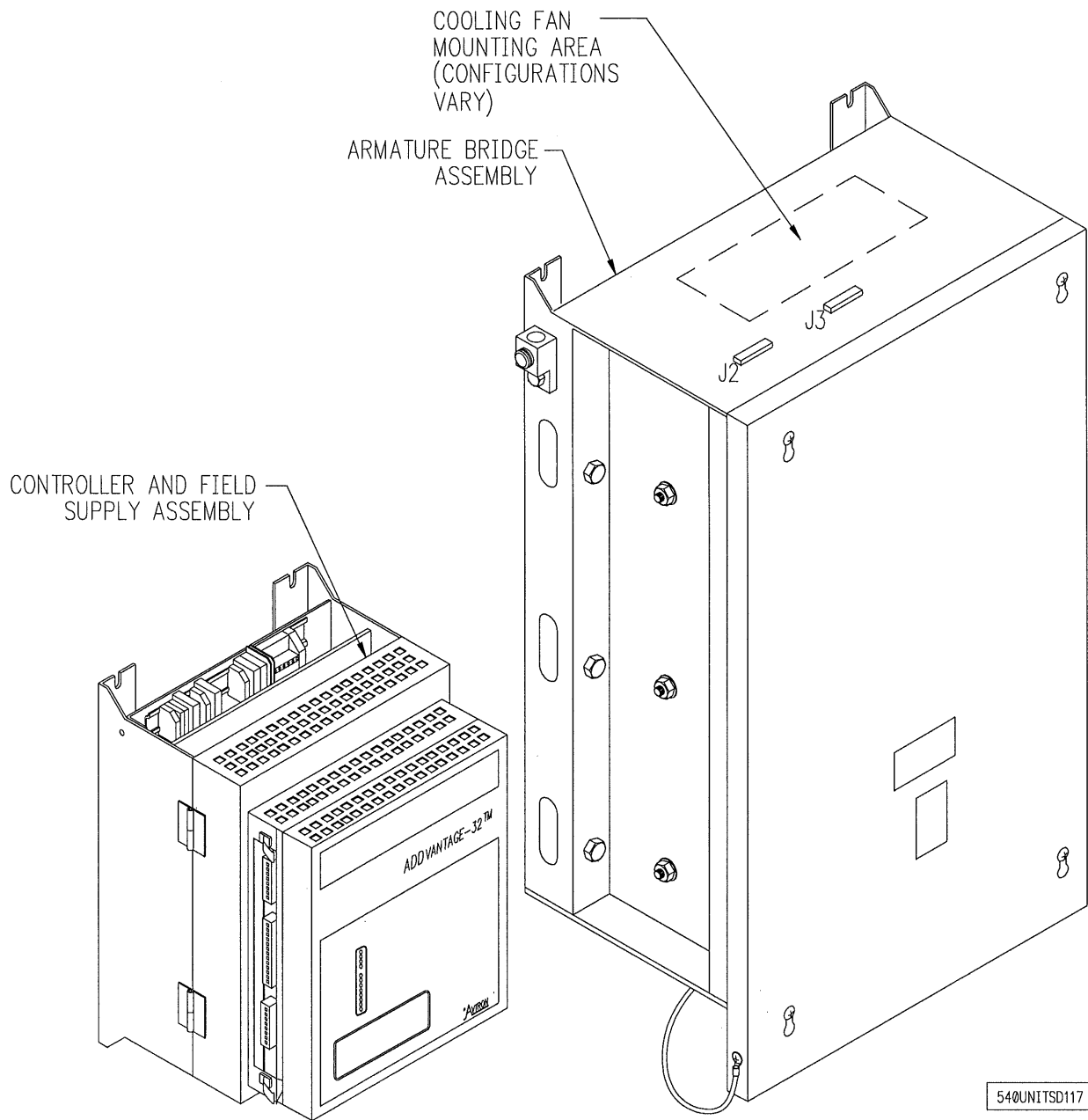


Figure 1-3. ADDvantage-32 AC to DC Power Converter  
(540, 850, 1550, and 3000 ADC)

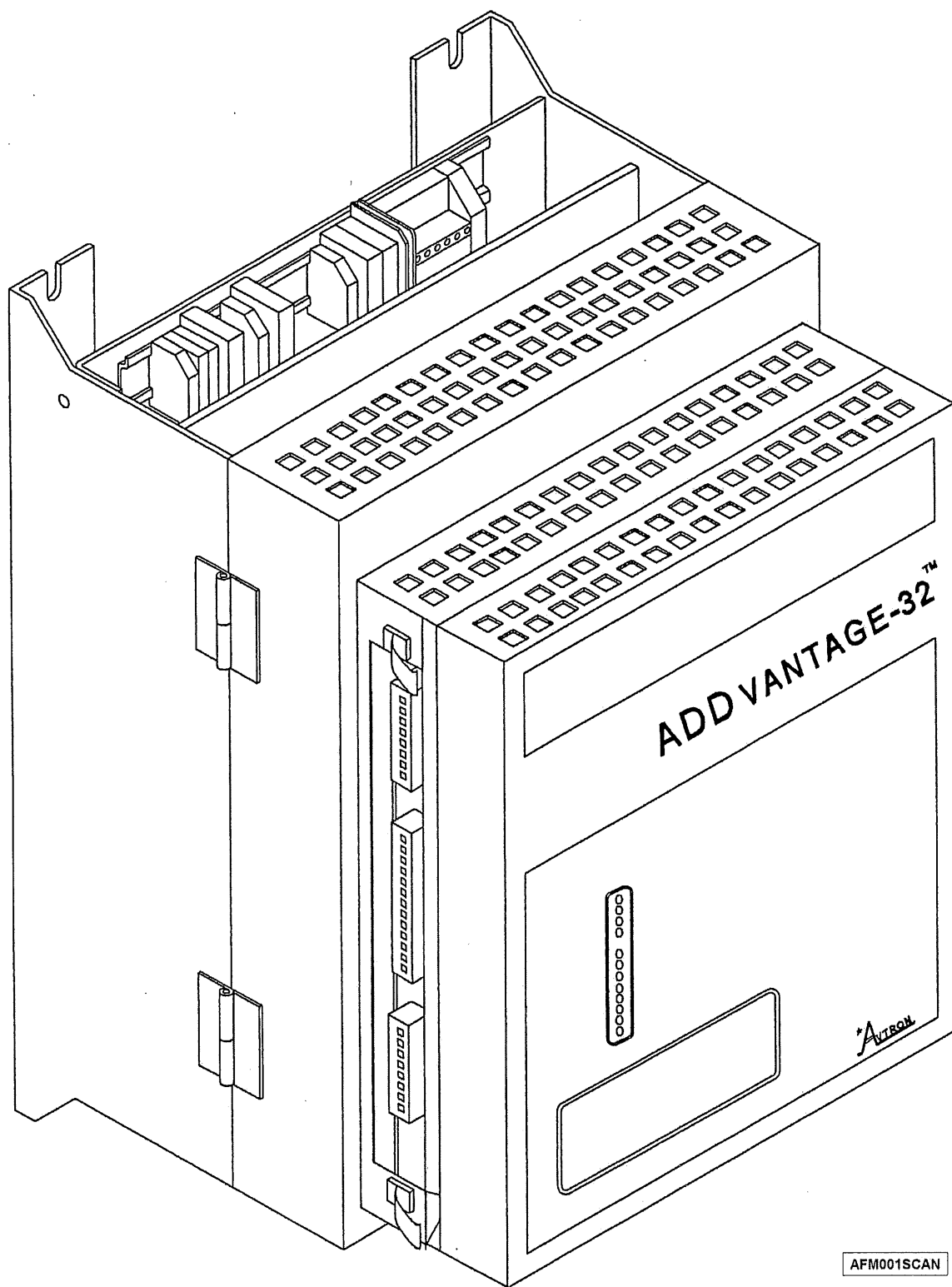


Figure 1-4. Advanced Firing Module (AFM)

The following components are contained in most of the hardware configurations. Hardware specific to a type will be indicated in the description. For example, power converters rated at 10 through 510 ADC and 550 amps have the SCR snubbers located on one board. Snubbers on units rated at 540, 850, 1550, and 3000 ADC are mounted directly on the SCR assembly. Advanced Firing Modules do not include snubbers.

## 1.2.1

MICROPROCESSOR BOARD

The MICROPROCESSOR BOARD (Figure 1-5) controls all functions including SCR firing, diagnostics, communications, and control block functions. The microprocessor board includes the following:

- The Intel i960, 32 bit superscaler microprocessor performs all ADDvantage-32 functions. The microprocessor computes multiple instructions per clock cycle, enabling the advanced features of the drive to function.
- A Flash PROM which stores the ADDvantage-32 application software program. Software upgrades can be accomplished over the serial link, eliminating the possibility of incorrectly installing or destroying integrated circuits.
- An EEPROM stores all of the calibration and configuration information, allowing all information to be retained during power loss and stored without battery-backup.
- Status LED's are mounted on the back of the microprocessor board. Except for the +5 POWER and PROCESSOR FAIL LED's, the LED's are software driven.
- The four-button keypad allows viewing or modification of all calibration, configuration, and running information.
- The 32-character alphanumeric display allows viewing of all ADDvantage-32 information. The 32 characters indicate English messages to the operator and represent the parameters in process units.

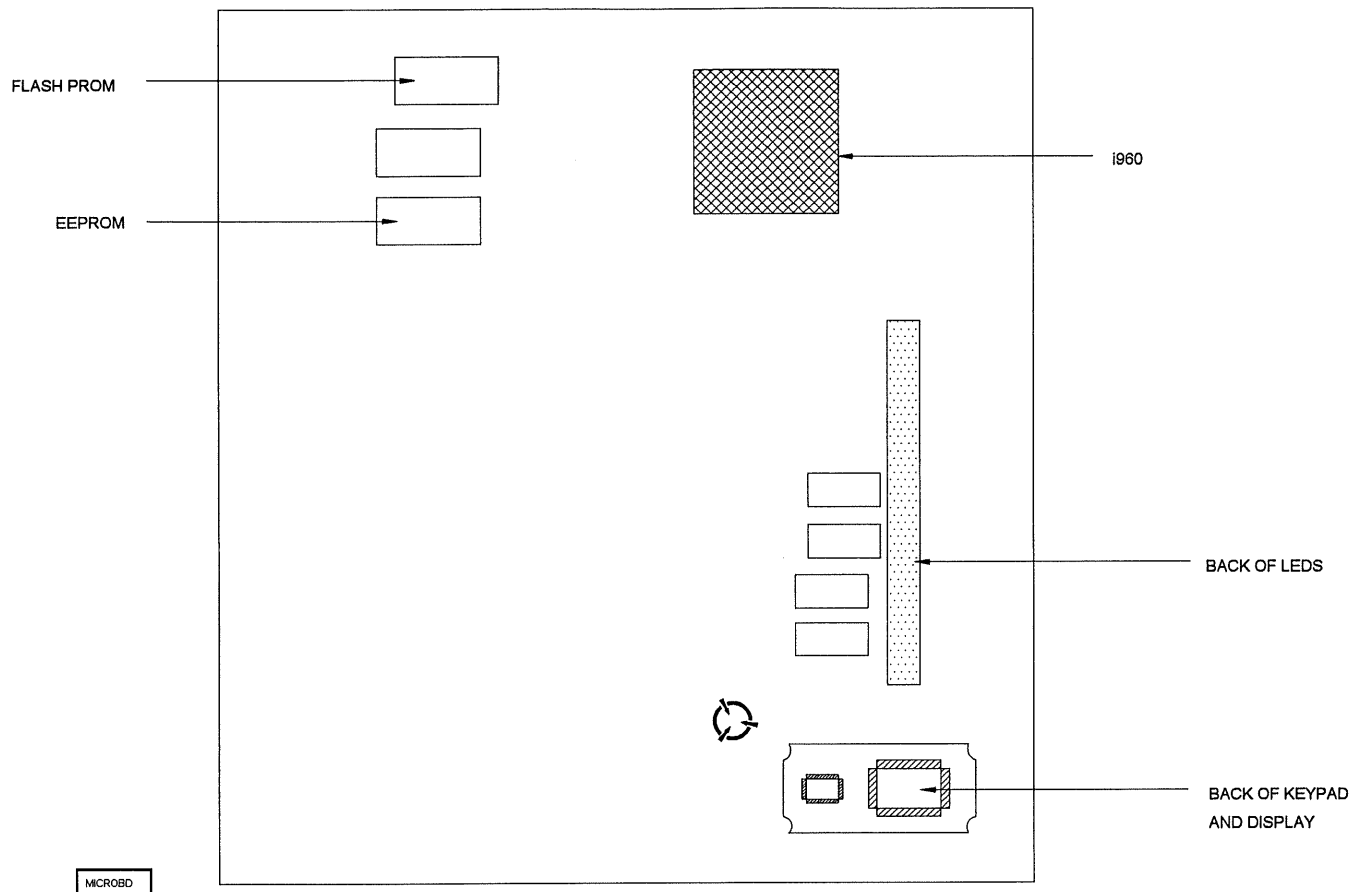


Figure 1-5. Microprocessor Board (A1)

Three microprocessor board options are currently available. Refer to Identification of Part Numbers for identification of a specific board.

- **ORIGINAL MICROPROCESSOR BOARD**

This is the original microprocessor board installed on early versions of the ADDvantage-32. It has been replaced by updated boards; however, original micro-processor boards are still available for replacement parts. Consult the factory for availability and delivery.

- **LOW MEMORY MICROPROCESSOR BOARD**

Low memory boards are used on ADDvantage-32's which do not require operation of the 802.4 LAN option or which do not use the new 692XXX or 694XXX software. If the LAN or latest software is required, a high memory board must be

used. The low memory microprocessor boards are used with non-LAN software numbers 690X0X, 691X0X, 690X1X, or 691X1X.

- HIGH MEMORY MICROPROCESSOR BOARD

High memory boards are used on ADDvantage-32's which use the 802.4 or 802.3 LAN option or which utilize the 692XXX or 694XXX software. This board can also be used on applications which do not use the LAN option. Software which is designed for LAN applications is number 691X5X. The high memory microprocessor board may also be used with non-LAN software numbers 691X0X or 691X1X.

### 1.2.2 SYSTEM PC BOARD

The SYSTEM BOARD (Figure 1-6) isolates user interconnections from the ADDvantage-32 circuitry and contains quick disconnect terminal blocks for user wiring. Several types of system boards are available as follows:

- MINI SYSTEM BOARD - Contains the smallest amount of I/O available. Features include:
  - (3) Analog Inputs
  - (1) Analog Output
  - (4) Digital Inputs
  - (1) RS485 Serial Link
- MAXI SYSTEM BOARD - Provides more I/O than the MINI version of this board. Features include:
  - (6) Analog Inputs
  - (4) Analog Outputs
  - (6) Digital Inputs
  - (4) Form C Digital Outputs
  - (2) Two-Phase Tachometer Inputs
  - (1) Buffered Tachometer Output
  - (1) RS485 Serial Link
- MAXI SYSTEM BOARD WITH 802.4 LAN - Contains the same I/O features as the standard MAXI board but also contains the LAN chip set to activate the 802.4 LAN.
- MAXI SYSTEM BOARD WITH FAX-32 BOARD - Same I/O features of the standard MAXI board with the addition of the FAX-32 piggyback board. The FAX-32 board provides the following additional I/O features:
  - (8) Digital Inputs
  - (2) Frequency Outputs capable of providing 200 to 20,200 Hz

- **MAXI SYSTEM BOARD w/FAX-32 AND 802.4 LAN** - Contains the same I/O features as the standard MAXI board and FAX-32 board with the addition of the 802.4 LAN chip set to enable LAN operation.

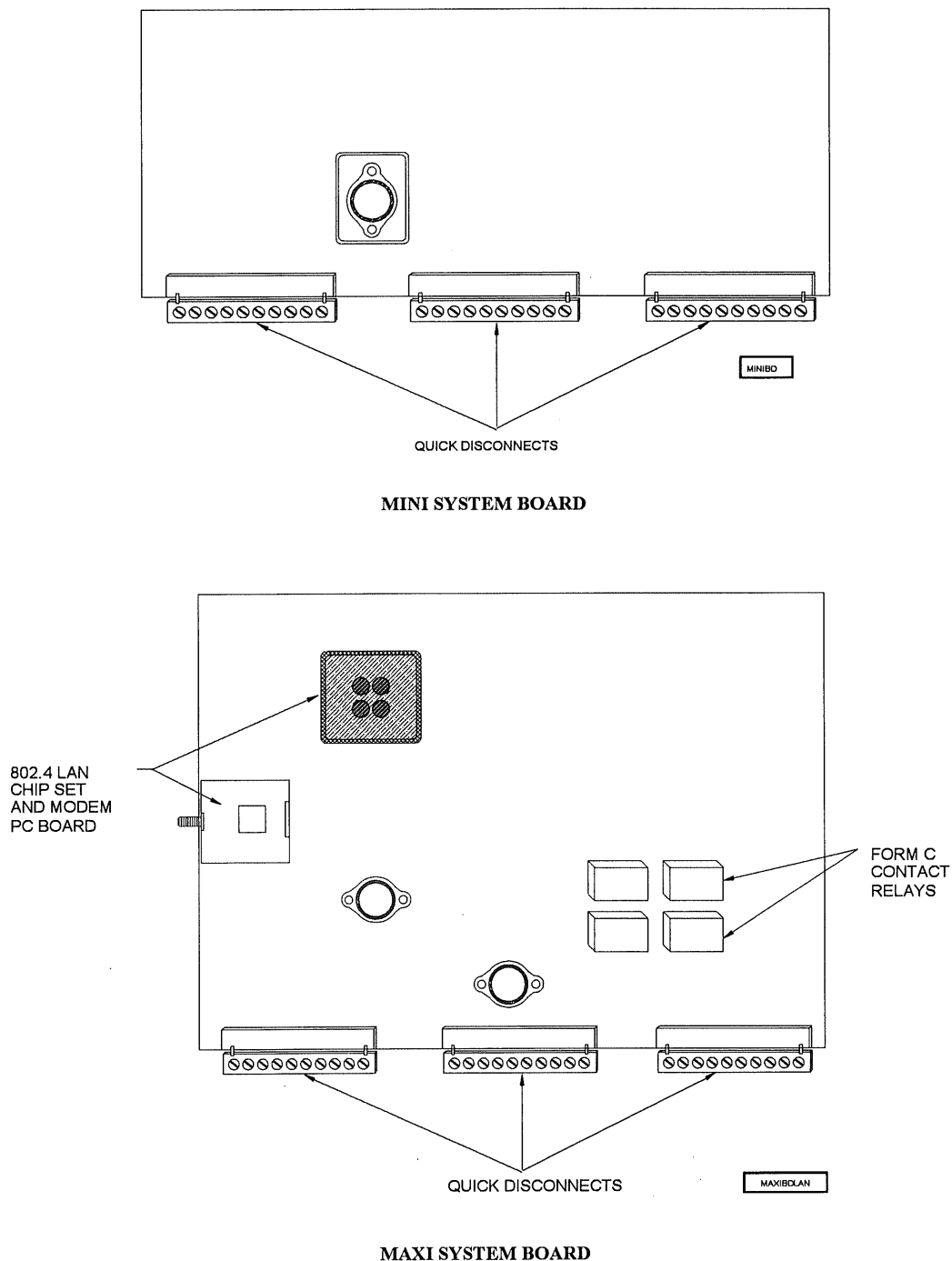


Figure 1-6. System PC Board (A2)



### 1.2.3 FAX-32 BOARD

The FAX-32 BOARD (Figure 1-7) is mounted piggyback to the Maxi System PC Board. Eight additional digital inputs are added to the maxi system board when the FAX-32 board is used. The FAX-32 board also provides a frequency output of 200 - 20,200 Hz. This frequency output can be used to cascade references.

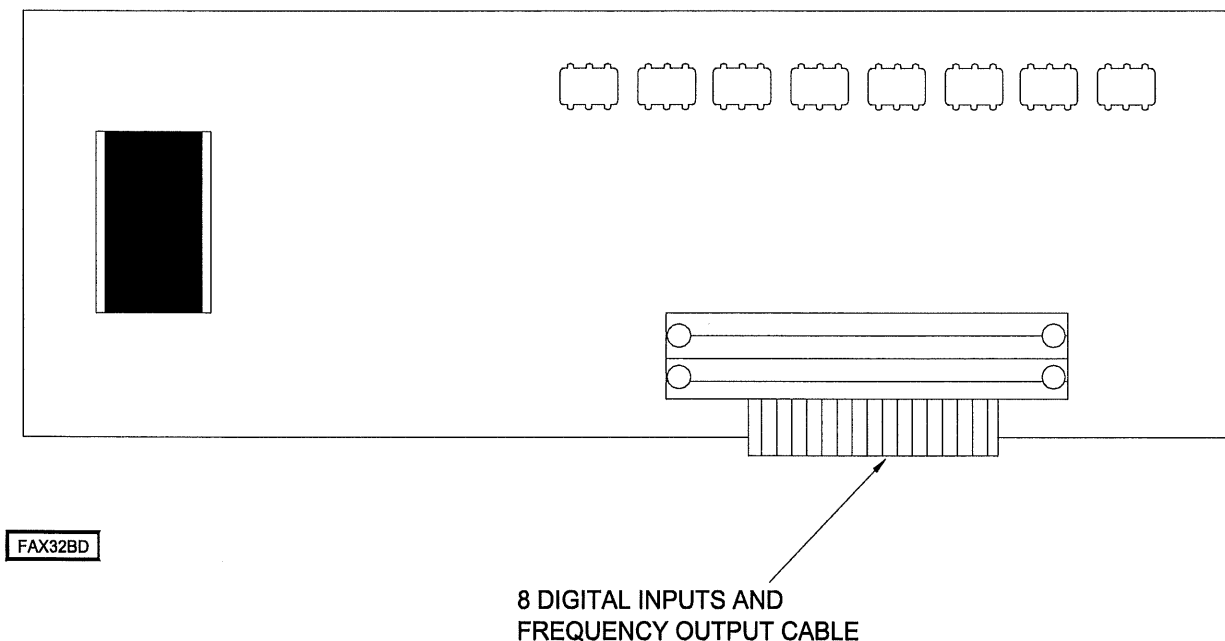


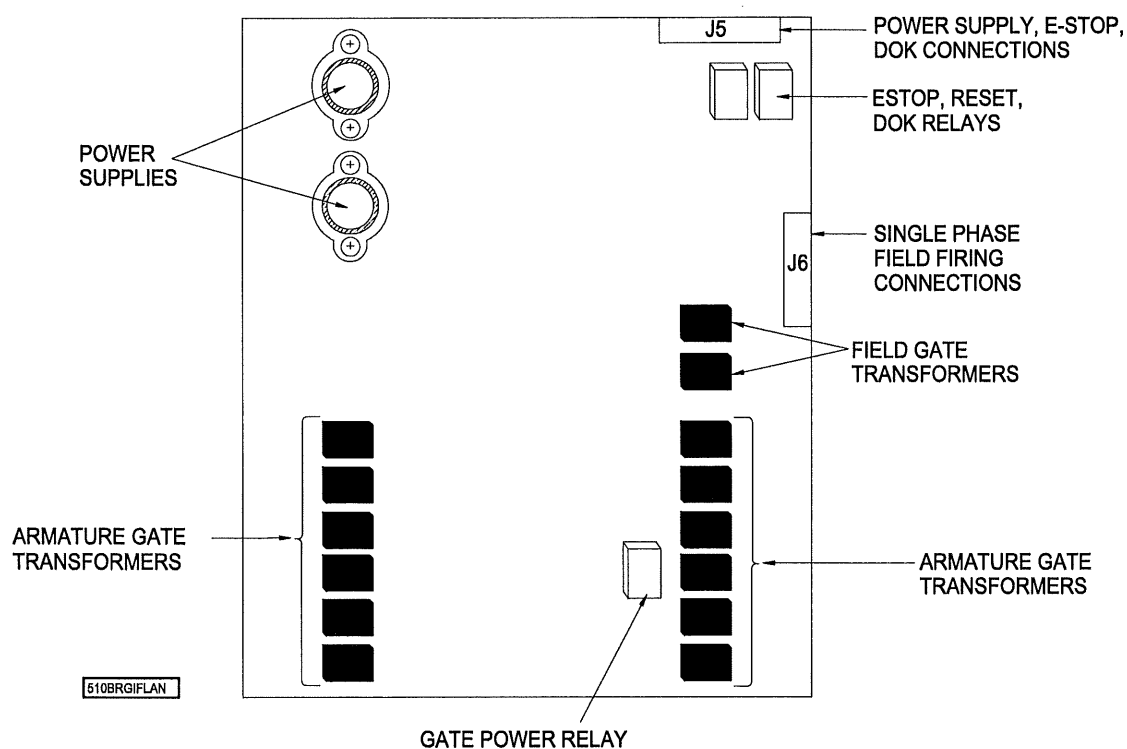
Figure 1-7. FAX-32 Board

### 1.2.4 BRIDGE INTERFACE BOARD

The BRIDGE INTERFACE BOARD (Figure 1-8) is an interface between the microprocessor board and the high power thyristor circuits. The main functional circuits on this board are as follows:

- Current Feedback Scaling and Isolation
- SCR (thyristor) Firing Circuitry and Isolation
- Power Supplies for all the Drive Boards
- ESTOP and Drive OK Relays
- SCR Heat Sink Temperature Feedback Circuitry
- Gate Power Relay
- Voltage Feedback Scaling and Isolation

# 10 THROUGH 510 AND 550 ADC CONVERTERS



# AFMs; 540, 850, 1550, AND 3000 ADC CONVERTERS

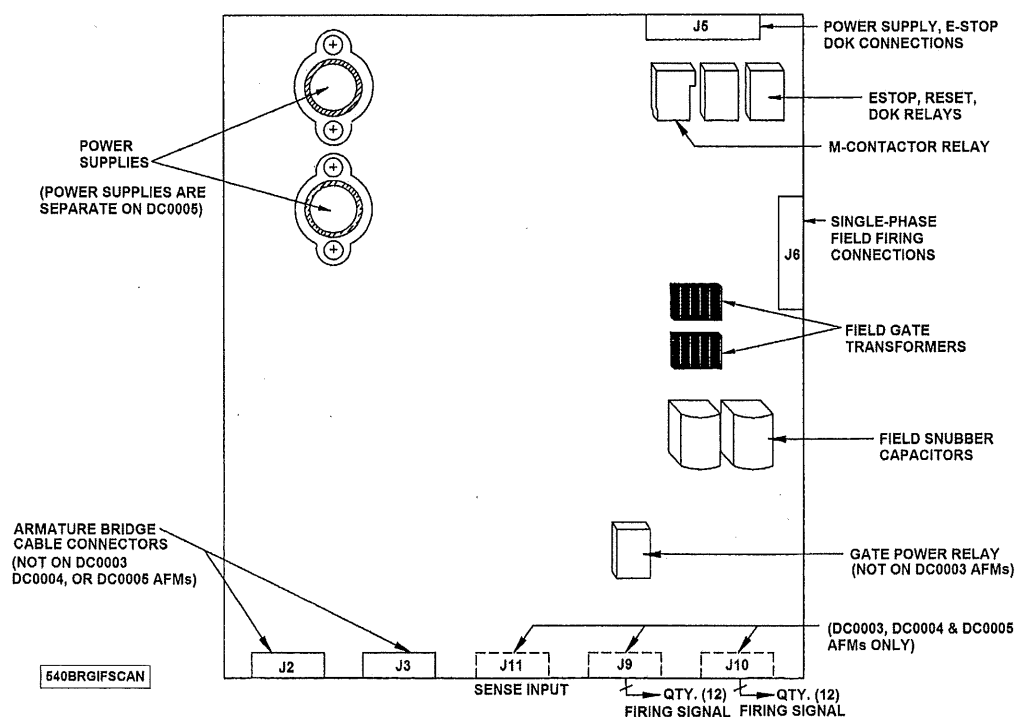


Figure 1-8. Bridge Interface Board (A3)

### 1.2.5 SNUBBER PC BOARD (10 through 510 and 550 ADC Power Converters only)

The SNUBBER BOARD (Figure 1-9) contains resistor/capacitor circuits for protection of the SCR's. They are placed on a board instead of across the SCR's so they are not misapplied when replacing an SCR. In units rated 540, 850, 1550, and 3000 ADC, the snubbers are mounted directly to the thyristor module assembly.

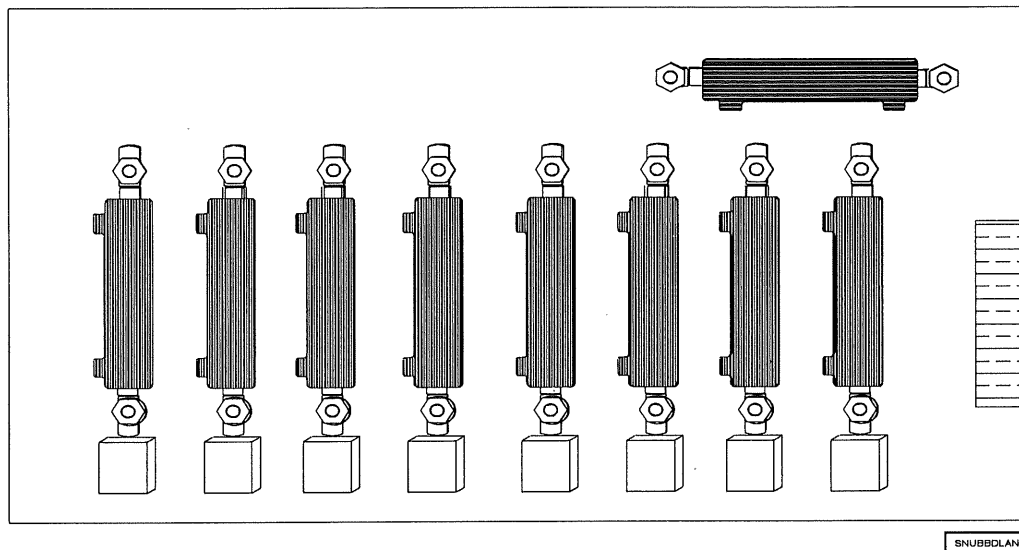


Figure 1-9. Snubber PC Board (A4)

### 1.2.6 DRIVE BASE ASSEMBLY (POWER CONVERTERS ONLY, 10 THROUGH 510 and 550 ADC)

The DRIVE BASE ASSEMBLY (Figure 1-10) on power converters rated 10 through 510 and 550 ADC contains all of the high voltage components. Heat generated by the SCR's is dissipated by the heat sinks included in the base assembly. The drive base assembly for 510 ADC and below is shown in Figure 1-10, and for 550 ADC in Figure 1-11. The base assemblies include the following:

#### Power Thyristor Bridge

The POWER THYRISTOR BRIDGE is a 6-pulse bridge which rectifies the incoming 3-phase voltage to DC. It permits the DC output voltage to be controlled, thereby controlling the speed of the connected DC motor. In the 4-quadrant, regenerative drive, two 6-pulse bridges are arranged in a back-to-back (non-circulating current) configuration which controls voltage and current for motoring and regenerating in both forward and reverse directions.

#### Shunt Field Supply

The SHUNT FIELD SUPPLY is a single phase thyristor/diode bridge which controls the excitation current to the motor's shunt wound field.

The AC supply comes from the 3-phase main supply. AC line fuses protect the converter against overcurrents caused by shorts.

#### Control Power Transformer

The control power transformer provides 115 VAC power for operation of the control circuitry and cooling fans. The only jumper on the drive is the control transformer configuration. Correctly jumper the transformer for 230 or 460 VAC incoming line-voltage.

The 550 amp drive base assembly includes optional configurations for 230, 460, or 575 VAC input. Refer to paragraph 6.6.4.

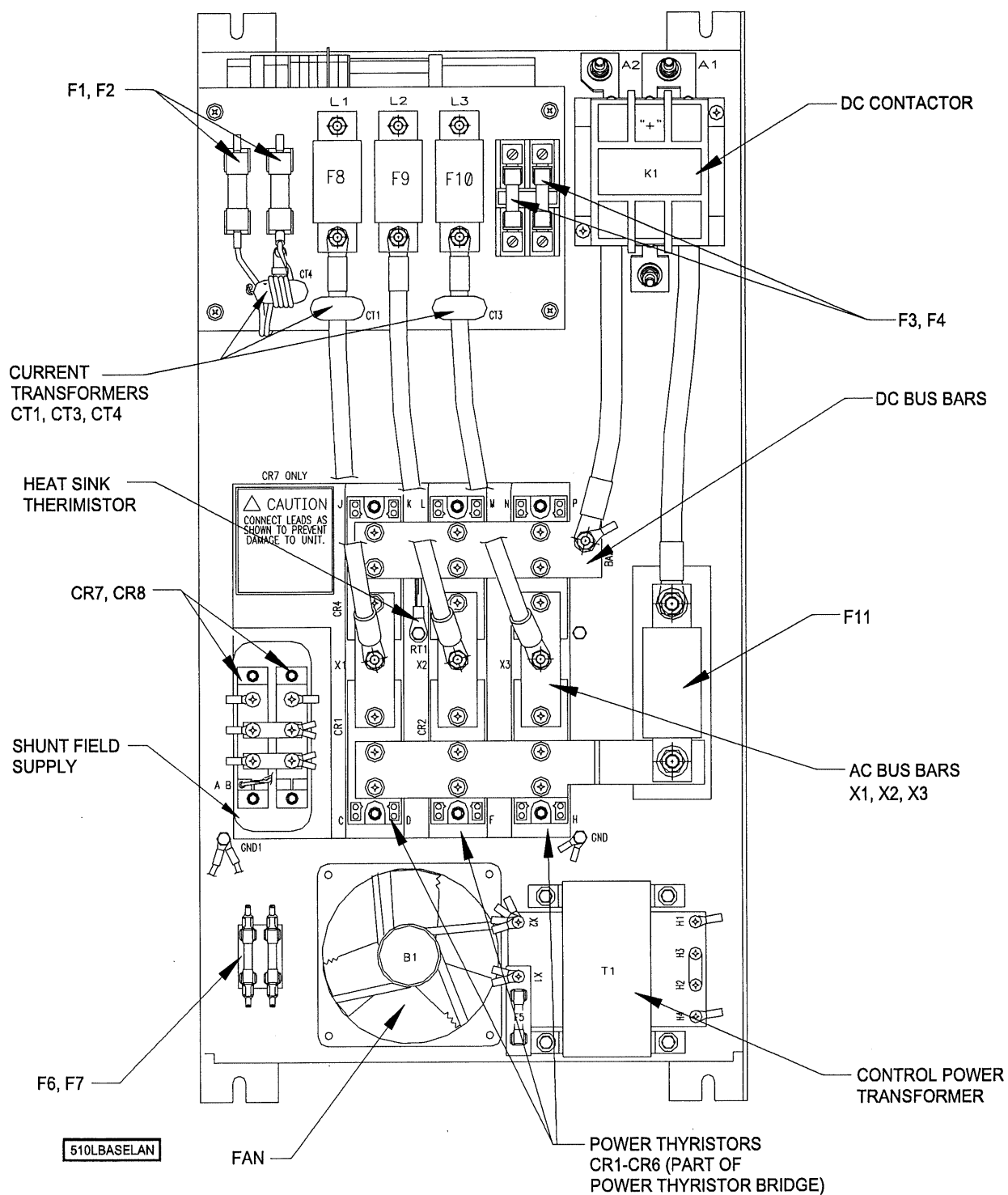


Figure 1-10. Drive Base Assembly (510 ADC and Below)

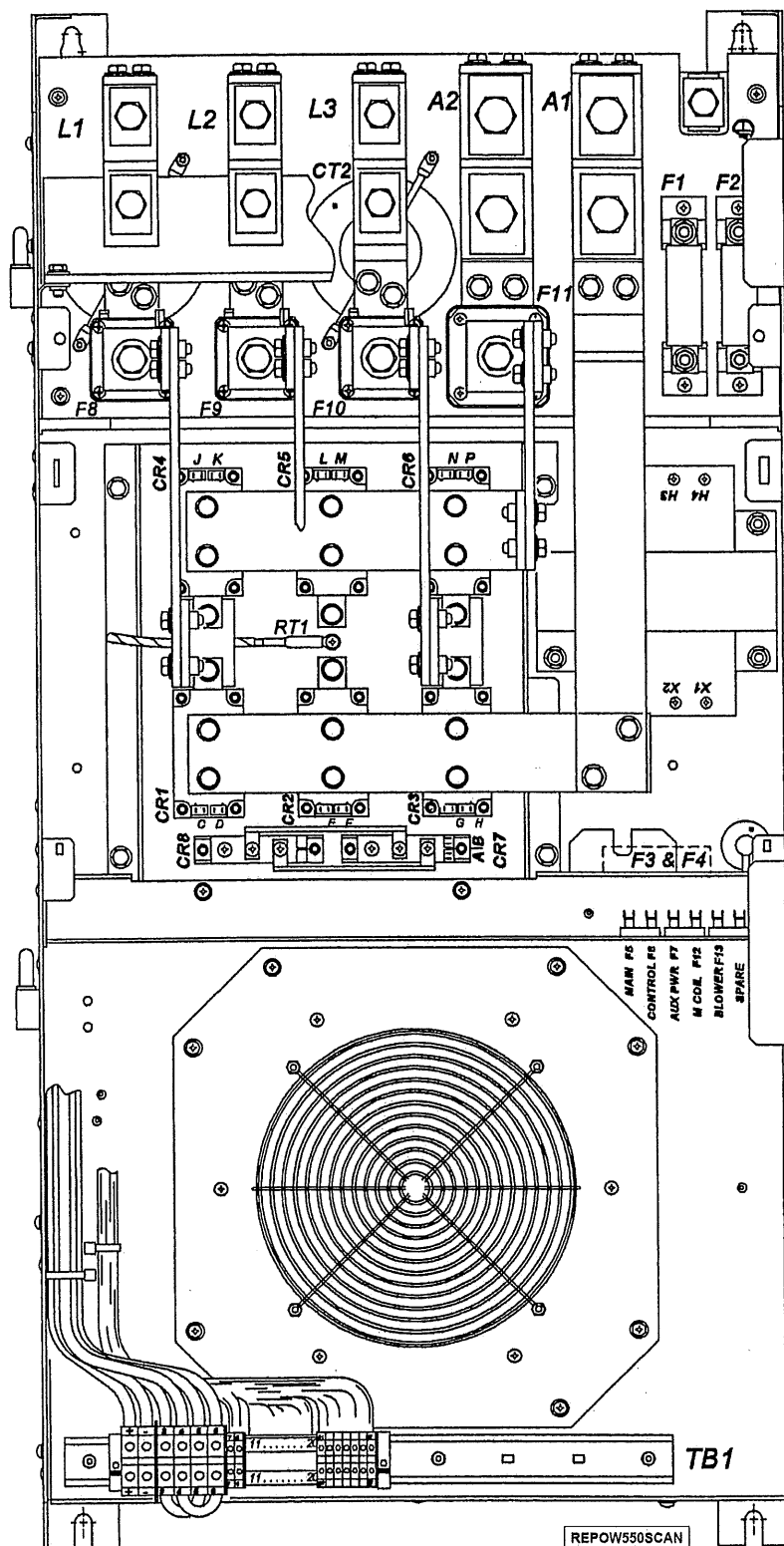


Figure 1-11. Drive Base Assembly (550 ADC)

### DC Contactor

A DC contactor is used to positively remove current from the motor armature. A dynamic braking (DB) pole may be provided as an option on all drives. Power converters may be purchased with or without contactors and with or without DB pole. The 510 ADC and above units have externally mounted contactors, while the 10-360 ADC versions are available with contactors mounted within the drive base assembly.

### Fusing (10 Through 510 and 550 ADC)

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#### **W A R N I N G**

Replace fuses only with same type and rating. Replacement with fuses other than those recommended may result in damage to the ADDvantage-32 and/or connected equipment, as well as severe injury or death to personnel.

\*\*\*\*\*

Fuses are located on the Drive Base Assembly for protection of the components. Refer to Section VII, Tables 7-8 and 7-9, for additional fuse replacement information.

- 3 AC line fuses (F8, F9, F10)
- 1 DC link fuse on regenerative units (F11)
- 2 Control transformer primary fuses (F3, F4)
- 2 Field supply AC line fuses (F1, F2)
- 3 Control power fuses (on 10 through 510 ADC units): F5, F6, F7
- 5 Control power fuses (on 550 ADC units): F5, F6, F7, F12, F13

### 1.2.7 FIELD CONTROLLER BASE ASSEMBLY (AFMs and 540, 850, 1550, and 3000 ADC Power Converters)

The FIELD CONTROLLER BASE ASSEMBLY is used on power converters rated 540, 850, 1550, and 3000 ADC as well as all AFMs. It contains the field supply components and the control electronics that operate the entire motor drive. (See Figure 1-12.) Heat generated by the field SCR's is dissipated by the heat sink contained in the base assembly. The base includes the Shunt Field Supply, fuses, bridge interface board, system board, and microprocessor board.

#### Shunt Field Supply

The SHUNT FIELD SUPPLY is a single phase thyristor/diode bridge which controls the excitation current to the motor's shunt wound field.

The AC supply comes from the 3-phase main supply. AC line fuses protect the converter against overcurrents caused by shorts.

Fusing (Refer to Section VII, Table 7-10, for fuse replacement information.)

Fuses contained in the field controller base assembly include: Field Supply AC line (F3, F4), Control Power Transformer Primary (rejection type) (F1, F2), Board Power (F5), Contactor Coil (F6), Cooling Blower (F7), and Auxiliary Power (F8). Fuses F1, F2, F6, and F7 are sized according to the external equipment that is being utilized with the ADDvantage-32 (i.e., contactors, control transformers, relays, etc.). These fuses must be supplied by the user or are provided in the optional auxiliary hardware kit which is available in addition to the standard DC motor drive.



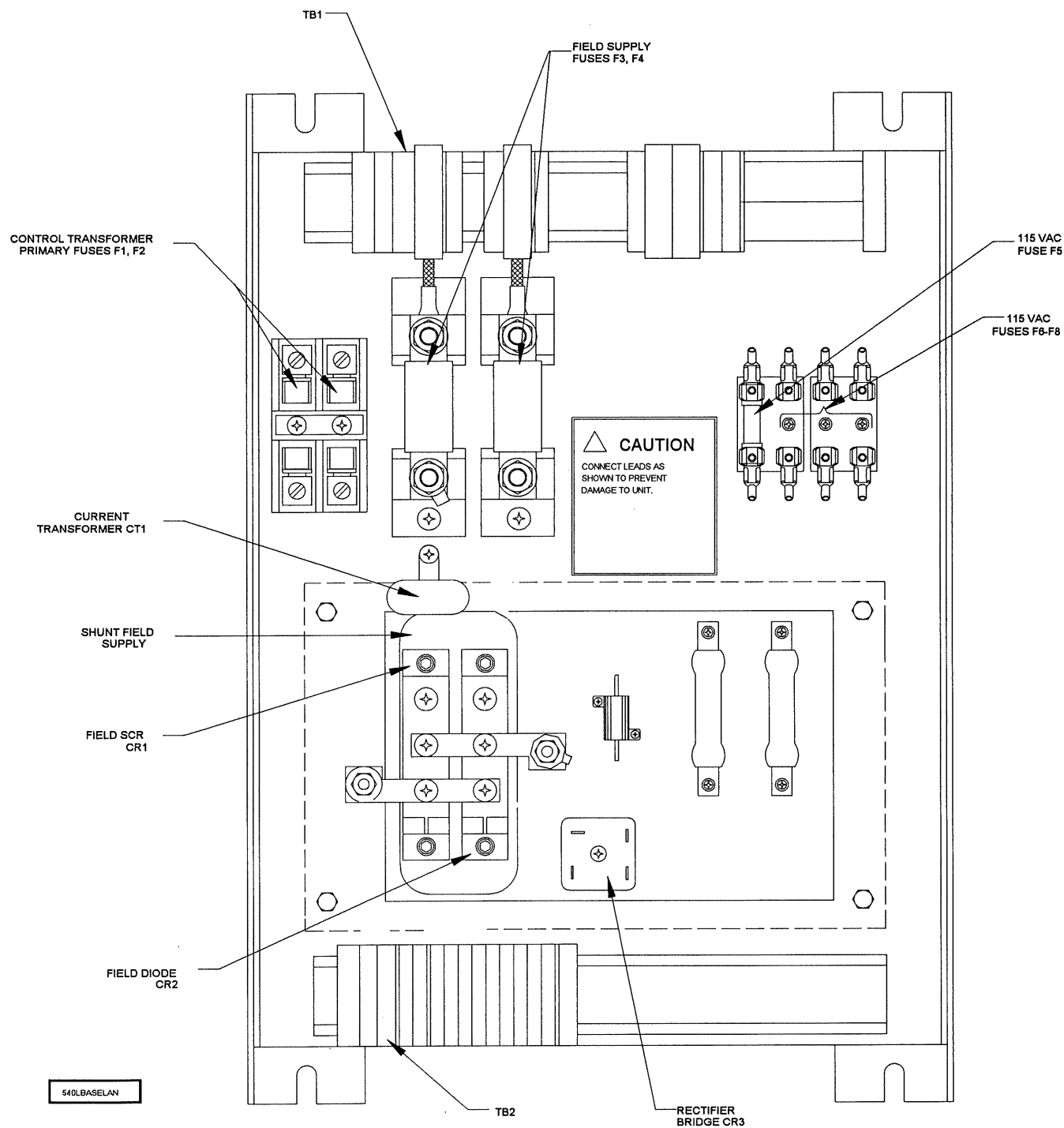


Figure 1-12. Field Controller Base Assembly  
(AFMs and 540, 850, 1550, 3000 ADC Power Converters)

1.2.8 ARMATURE BRIDGE ASSEMBLY (540, 850, 1550, and 3000 ADC power converters only)

The ARMATURE BRIDGE ASSEMBLY contains the high voltage armature control components as shown in Figure 1-13 and Figure 1-14. The chassis supports the thyristor module assemblies, bus bars, fuses, and current transformers. Blowers on the top of the unit generate airflow across the heatsinks for heat dissipation. The armature bridge assembly contains the thyristor modules, firing circuitry, current sensing, blowers (on 540 and 850 amp drives), and fusing to protect the thyristors.

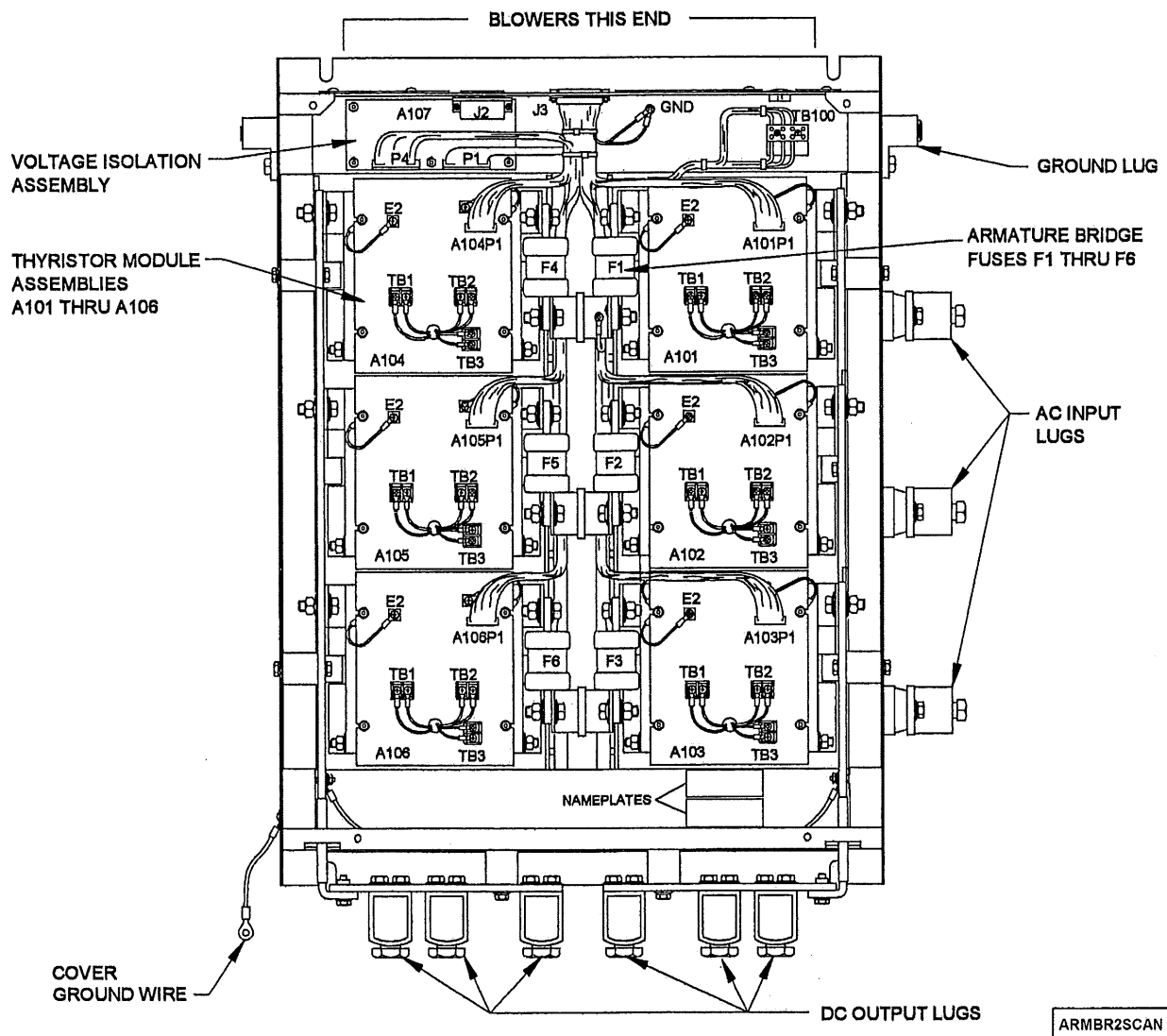


Figure 1-13. Armature Bridge Assembly  
(540 and 850 Amp Power Converters Only)

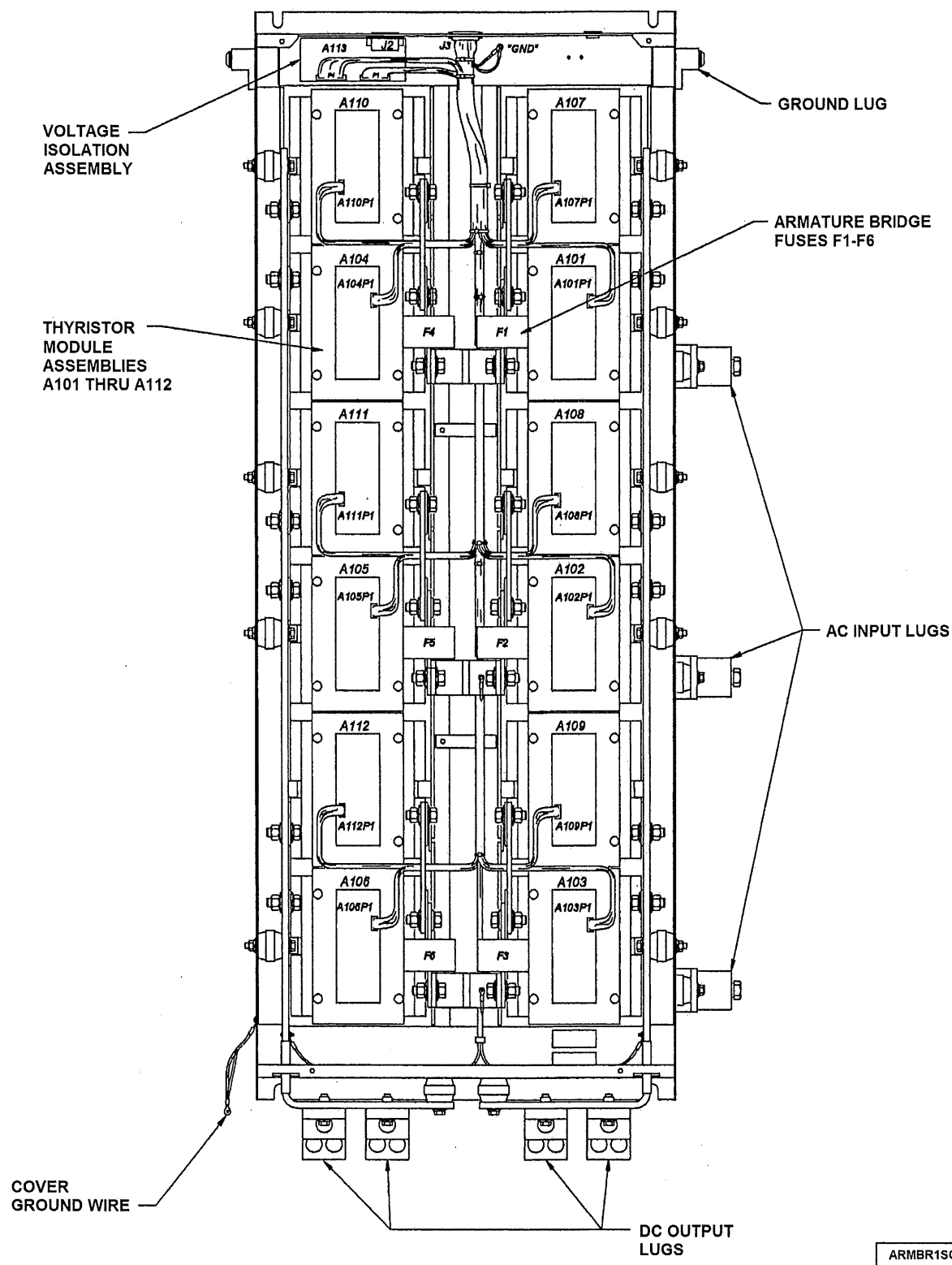


Figure 1-14. Armature Bridge Assembly  
(1550 Amp and 3000 Amp Power Converters Only)

## 1.2.9

THYRISTOR MODULE ASSEMBLY (540 ADC, 850 ADC, 1550 ADC, and 3000 ADC Power Converters)

The THYRISTOR MODULE ASSEMBLY contains the SCR(s), firing/ snubber board, air baffle, and bus bars. (Refer to Figures 1-15 and 1-16.) The 540 amp and 850 amp THYRISTOR MODULE ASSEMBLY contains one SCR for non-regenerative type bridges or two SCR's for regenerative type bridges.

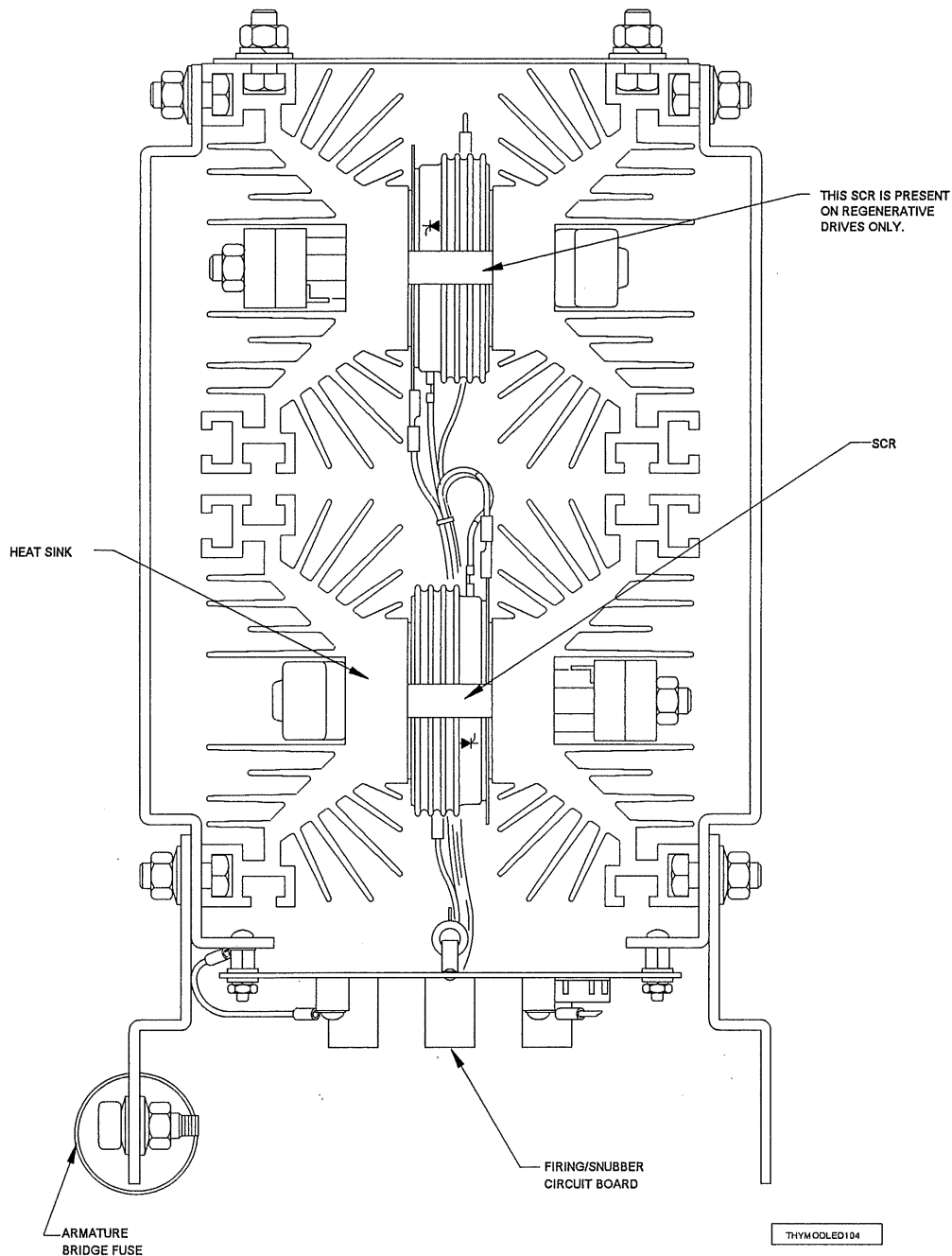


Figure 1-15. Thyristor Module Assembly  
(540 and 850 Amp, Regen. Power Converters Only)

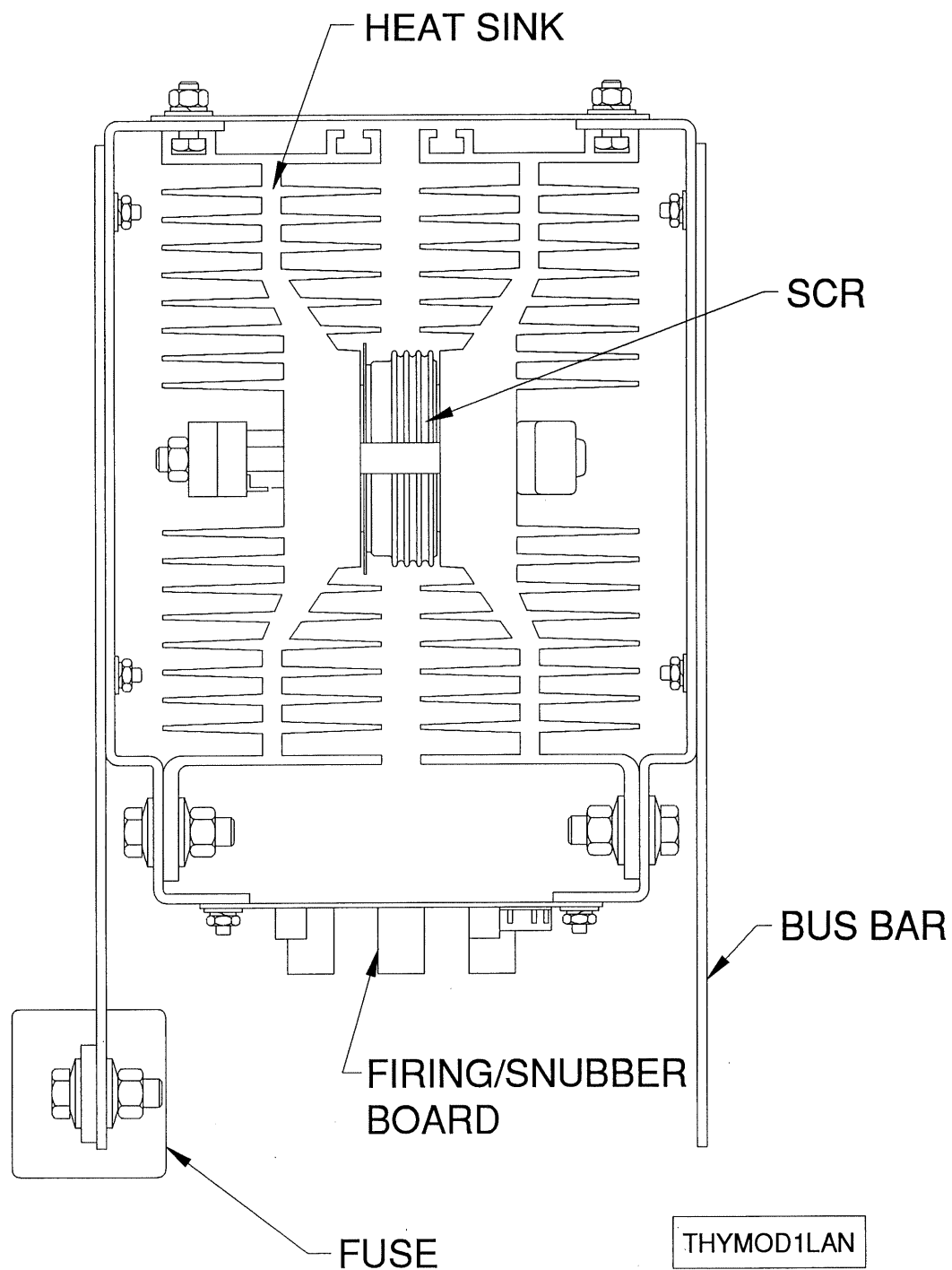


Figure 1-16. Thyristor Module Assembly  
(1550 Amp and 3000 Amp Power Converters Only)

## 1.3 SOFTWARE FEATURES

The setup of an ADDvantage-32 is done through calibrating and configuring the various parameters. No programming is necessary. The calibration parameters are constant numbers that the user enters into the drive. An example would be the maximum line speed or an analog input scaling factor. The configuration parameters direct where an input comes from. An example would be the speed reference coming from the first frequency input instead of a calibration number.

There are two real time data tables in the ADDvantage-32. All ongoing information is stored in these tables. The values can then be used for various functions or be viewed or recorded. The first data table is for bit information such as a drive OK bit. The second is for floating point data such as actual motor speed.

The software is also broken down into two parts. The first part is the core software which consists of all low level routines including:

- I/O scanning - SCR firing - Diagnostics -
- Serial link communications - LAN communications -
- Keypad protocol - Inner armature and field current loops

The core has its own calibration and configuration parameters and outputs its data to the real time data tables. See Section III for a detailed description of the base software.

The second part of the software is the application code. This portion is programmed into software control blocks. The blocks are then connected together to form a personality such as speed/tension or center driven winder control. The inputs of the blocks can come from the real time data tables, calibration parameter, or a configuration parameter. The outputs of the blocks always go to the real time data tables where they can be viewed or used as inputs to other blocks. Chapter IV describes the library of blocks that can be used in a particular application. Appendices A through D explain all the interconnections between the blocks to form the application for the software part number of this manual. Other than the Appendices, this manual is the same for all ADDvantage-32 drives.

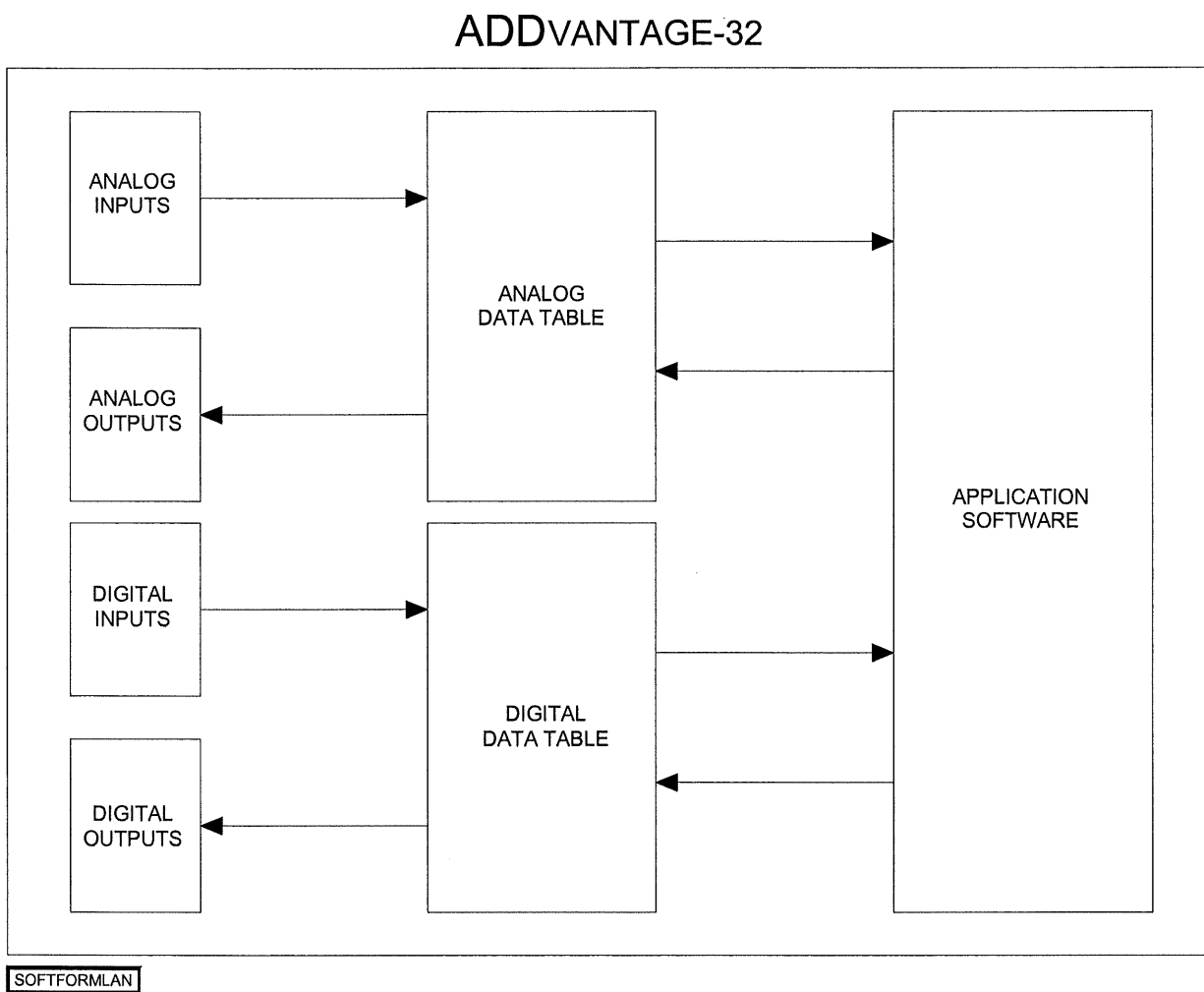


Figure 1-17. Software Format

## 1.4

**IDENTIFICATION OF PART NUMBERS**

The part numbering of the ADDvantage-32 consists of two separate numbers. The hardware part number is located on nameplates found on both the inside and outside of the unit and reflects the hardware configuration of the ADDvantage-32. The software part number, as well as the version number, identifies the application software used with the ADDvantage-32 hardware.

**HARDWARE PART NUMBER (EXAMPLE)**

MODEL TYPE ALWAYS DC		SYSTEM I.D. AND AMP RATING				QUAD- RANTS/ AFM FIELD		SYSTEM BOARD	OPTION 1	OPTION 2	MICRO- PROCESSOR BOARD TYPE	
D	C	0	0	3	0	4	A	0	0		C	

**SOFTWARE PART NUMBER (EXAMPLE)**

6-DIGIT SOFTWARE PART NUMBER						VERSION NUMBER		
6	9	2	0	0	2	V	2	5

Figure 1-18. Part Number Breakdown



1.4.1 HARDWARE PART NUMBER BREAKDOWN

**MODEL TYPE** defines the type of armature voltage to be controlled (always DC).

**SYSTEM I.D. AND AMP RATING**

SELECTION	DESCRIPTION
0001	Advanced Firing Module (AFM)
0002	AFM Without Field Supply
0003	AFM for 24 SCR Firing
0004	AFM for 24 SCR Firing Without Field Supply
10	10 ADC Armature, 3 ADC Field Supply Power Converter
30	30 ADC Armature, 3 ADC Field Supply Power Converter
56	56 ADC Armature, 6 ADC Field Supply Power Converter
110	110 ADC Armature, 6 ADC Field Supply Power Converter
180	180 ADC Armature, 12 ADC Field Supply Power Converter
280	280 ADC Armature, 12 ADC Field Supply Power Converter
360	360 ADC Armature, 12 ADC Field Supply Power Converter
510	510 ADC Armature, 12 ADC Field Supply Power Converter
540	540 ADC Armature, 12 ADC Field Supply Power Converter
541	540 ADC Armature, 24 ADC Field Supply* Power Converter
542	540 ADC Armature, 48 ADC Field Supply* Power Converter
550	550 ADC Armature, 12 ADC Field Supply Power Converter
551	550 ADC Armature, 24 ADC Field Supply Power Converter
552	550 ADC Armature, 48 ADC Field Supply Power Converter
850	850 ADC Armature, 12 ADC Field Supply* Power Converter
851	850 ADC Armature, 24 ADC Field Supply* Power Converter
852	850 ADC Armature, 48 ADC Field Supply* Power Converter
1550	1550 ADC Armature, 12 ADC Field Supply* Power Converter
1551	1550 ADC Armature, 24 ADC Field Supply* Power Converter
1552	1550 ADC Armature, 48 ADC Field Supply* Power Converter
2500	2500 ADC Armature, 12 ADC Field Supply* Power Converter
2501	2500 ADC Armature, 24 ADC Field Supply* Power Converter
2502	2500 ADC Armature, 48 ADC Field Supply* Power Converter
3000	3000 ADC Armature, 12 ADC Field Supply* Power Converter
3001	3000 ADC Armature, 24 ADC Field Supply* Power Converter
3002	3000 ADC Armature, 48 ADC Field Supply* Power Converter

\*Power converters rated 540 ADC, 850 ADC, 1550 ADC, and 3000 ADC include a control unit separate from the armature bridge assembly. These units contain the motor field bridge and are available in various ratings.

**QUADRANTS/AFM FIELD****Power Converters**

SELECTION	DESCRIPTION
2	Non-Regenerative Armature Bridge*. 240 or 500 VDC, selectable.
4	Regenerative Armature Bridge. 240 or 500 VDC, selectable, plus 650 VDC on DC0550
A	Same as "2" except 700 VDC can also be selected on 1550 and 3000A units
B	Same as "4" except 700 VDC can also be selected on 1550 and 3000A units
N	Non-Regenerative Modular Design Armature Bridge**
M	Regenerative Modular Design Armature Bridge**

\*Non-regenerative options are only available on units rated 540, 850, 1550, and 3000 ADC.

Software parameters allow reverse bridge operation to be disabled on all units.

\*\*Available on 540, 850, 1550, and 3000 ADC.

**Advanced Firing Modules**

SELECTION	DESCRIPTION
0	12 Amp Field
1	24 Amp Field
2	48 Amp Field
3	6 Amp Field
4	12 Amp Field (4 SCR)
5	24 Amp Field (4 SCR)
6	48 Amp Field (4 SCR)

**SYSTEM BOARDS**

SELECTION	DESCRIPTION
A	MINI System Board
B	MAXI System Board
C	MAXI With 802.4 LAN
D	MAXI With FAX-32
E	MAXI With 802.4 LAN and FAX-32

Refer to Section 1.5 of this manual for additional system board descriptions.

**OPTION 1**

On AFM systems, this block identifies a customer-specific application.

SELECTION	DESCRIPTION
0	Non-listed
L	UL Listed
N	Modular design used in conjunction with Options 0, 2, and 3 of Option 2. When specifying this feature, Option 2 must also be specified. It can only be specified on units rated 10 through 510 and 550 ADC.
4	4 SCR Field Supply. Available on 540, 850, 1550, and 3000 ADC power converters.

**OPTION 2**

On AFM systems, this block identifies a customer-specific application.

SELECTION	DESCRIPTION
0	Right side AC input (540, 850, 1550, and 3000 ADC)
1	Left side AC input (540, 850, 1550, and 3000 ADC)
0	Specified with Option N of Option 1 with no contactor provided*
2	Specified with Option N of Option 1 for a contactor without DB pole*
3	Specified with Option N of Option 1 for a contactor with DB pole*

\*Only available on units rated 10 through 510 ADC and 550 ADC.

**MICROPROCESSOR BOARDS**

SELECTION	DESCRIPTION
A	Original ADDvantage-32 Microprocessor Board
B	Low Memory Microprocessor Board
C	High Memory Microprocessor Board - STANDARD
702	Standard Drive AFM
703	Winder Drive AFM

Refer to Section 1.2.1 of this manual for additional microprocessor board descriptions.

#### 1.4.2 SOFTWARE PART NUMBER BREAKDOWN

The software part number is a six-digit number which represents the application software installed in the ADDvantage-32. Several different types are available including a standard speed regulator with tension (P/N 692002) and a center driven winder (P/N 692003). Most applications can be covered by the two application programs described. Other application software is available. To obtain a list or to discuss custom software applications, consult the factory.

#### **NOTE**

A two-digit version number is also required. If a specific version is not referenced, the latest version will be supplied.

## 1.5 SPECIFICATIONS

Please note that some of the following specifications are not pertinent to all models.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS

DESCRIPTION		SPECIFICATION*		
Input Voltage to Transformer		3-Phase primary windings to standard voltages (Phase rotation insensitive)		
Transformer Output to Drive**		3-Phase, 230 or 460 VAC (nominal), except 550 ADC Drive only - 230, 460, or 575 VAC (nominal)		
Maximum Currents				
Drive P/N	HP 240/500/700 VDC	Armature Output	Input Current	Field Output
DC0010	2/5	10 Amps DC	11 Amps AC	3 Amps DC
DC0030	7.5/15	30 Amps DC	28 Amps AC	3 Amps DC
DC0056	15/30	56 Amps DC	49 Amps AC	6 Amps DC
DC0110	30/60	110 Amps DC	95 Amps AC	6 Amps DC
DC0180	50/100	180 Amps DC	155 Amps AC	12 Amps DC
DC0280	75/150	280 Amps DC	240 Amps AC	12 Amps DC♦
DC0360	100/200	360 Amps DC	310 Amps AC	12 Amps DC♦
DC0510	150/300	510 Amps DC♦♦	416 Amps AC	12 Amps DC♦
DC0540	150/300	540 Amps DC	440 Amps AC	12 Amps DC
DC0541	150/300	540 Amps DC	440 Amps AC	24 Amps DC
DC0542	150/300	540 Amps DC	440 Amps AC	48 Amps DC
DC0550	150/300/400	550 Amps DC	459 Amps AC	12 Amps DC
DC0551	150/300/400	550 Amps DC	470 Amps AC	24 Amps DC
DC0552	150/300/400	550 Amps DC	488 Amps AC	48 Amps DC
DC0850	250/500	850 Amps DC	700 Amps AC	12 Amps DC
DC0851	250/500	850 Amps DC	700 Amps AC	24 Amps DC
DC0852	250/500	850 Amps DC	700 Amps AC	48 Amps DC
DC1550	500/1000/1250	1550 Amps DC	1265 Amps AC	12 Amps DC
DC1551	500/1000/1250	1550 Amps DC	1265 Amps AC	24 Amps DC
DC1552	500/1000/1250	1550 Amps DC	1265 Amps AC	48 Amps DC
DC3000	900/1800/2500	3000 Amps DC	2460 Amps AC	12 Amps DC
DC3001	900/1800/2500	3000 Amps DC	2470 Amps AC	24 Amps DC
DC3002	900/1800/2500	3000 Amps DC	2490 Amps AC	48 Amps DC

\* Additional Specifications are located in the supplemental drawing package.

\*\* An isolation transformer or line reactor is required when applying each ADD-32 drive to a power distribution system. A total impedance from the power distribution source to the drive input in the range of 3% to 6% is required. Total KVA rating of transformer should not exceed 3 times the drive rating. If a drive isolation transformer is supplying power to multiple drives, then each drive must have a line reactor. If a combination of isolation transformer and line reactor is used, the reactor should contribute the majority of the line impedance (better than 2:1 ratio). Provided that each ADD-32 has the proper source impedance, any number of drives or frame sizes can be connected to a common power source. Connection of any power converter to a transformer with primary rating of 2300 VAC or more may require additional input line conditioning at the power converter to prevent damage to electrical components. Contact Avtron Industrial Automation, Inc., for assistance when this is required.

♦ A 24 amp field option is available on drives with a 12 amp field.

♦♦ Consult factory for overload rating.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

DESCRIPTION	SPECIFICATION*																								
Line Voltage Variation	+/-10% of nominal																								
Line Frequency Range	43 to 63 Hz																								
Armature Voltage Range																									
	<table><tr><th>Drive P/N</th><th>Armature Current</th><th>Voltage</th></tr><tr><td>DC0010-0510-XXXX</td><td>10 through 510 ADC</td><td>240, 500 VDC</td></tr><tr><td>DC054X-XXXX</td><td>540 ADC</td><td>240, 500 VDC</td></tr><tr><td>DC055X-XXXX</td><td>550 ADC</td><td>240, 500, 650 VDC</td></tr><tr><td>DC085X-XXXX</td><td>850 ADC</td><td>240, 500 VDC</td></tr><tr><td>DC155X - 2XXX 4XXX</td><td>1550 ADC</td><td>240, 500 VDC</td></tr><tr><td>DC155X - AXXX BXXX</td><td>1550 ADC</td><td>240, 500, 700 VDC</td></tr><tr><td>DC300X - XXXX</td><td>3000 ADC</td><td>240, 500, 700 VDC</td></tr></table>	Drive P/N	Armature Current	Voltage	DC0010-0510-XXXX	10 through 510 ADC	240, 500 VDC	DC054X-XXXX	540 ADC	240, 500 VDC	DC055X-XXXX	550 ADC	240, 500, 650 VDC	DC085X-XXXX	850 ADC	240, 500 VDC	DC155X - 2XXX 4XXX	1550 ADC	240, 500 VDC	DC155X - AXXX BXXX	1550 ADC	240, 500, 700 VDC	DC300X - XXXX	3000 ADC	240, 500, 700 VDC
Drive P/N	Armature Current	Voltage																							
DC0010-0510-XXXX	10 through 510 ADC	240, 500 VDC																							
DC054X-XXXX	540 ADC	240, 500 VDC																							
DC055X-XXXX	550 ADC	240, 500, 650 VDC																							
DC085X-XXXX	850 ADC	240, 500 VDC																							
DC155X - 2XXX 4XXX	1550 ADC	240, 500 VDC																							
DC155X - AXXX BXXX	1550 ADC	240, 500, 700 VDC																							
DC300X - XXXX	3000 ADC	240, 500, 700 VDC																							
Armature Current Range	33% to 100% drive rating (Below 50% bridge self test may need to be disabled.)																								
Armature Control	four quadrant: fully regenerative two quadrant: non-regenerative																								
Armature Overload Capacity	150% for 60 seconds																								
Field Current Regulation	Continuous throughout speed range																								
Mini System Board	(3) analog inputs, (1) analog output, (4) digital inputs, (1) RS485 Serial Link																								
Maxi System Board	(6) analog inputs, (4) analog outputs, (6) digital inputs, (4) digital outputs, (2) two-phase tach inputs, (1) buffered tach output, (1) RS485 Serial Link or (1) 802.4 LAN Interface																								

\* Additional Specifications are located in the supplemental drawing package.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

DESCRIPTION	SPECIFICATION*																				
FAX-32 Board	(8) digital inputs, (2) identical frequency outputs, 200 - 20,200 Hz frequency range, Duty cycle of 50% $\pm 1\%$ , 50 mA I <sub>max</sub> , V <sub>out</sub> of 5V differential, $\pm .017$ commanded accuracy, $\pm .017$ commanded resolution																				
Digital Input Ratings																					
<table><tr><td>Input Voltage (DC)</td><td>MIN</td><td>NOM</td><td>MAX</td></tr><tr><td>Common Mode (Logic High) (Logic Low)</td><td>10 VDC -1 VDC</td><td>24 VDC 0 VDC</td><td>30 VDC 9 VDC</td></tr><tr><td>Common Mode Rejection</td><td></td><td></td><td>100 VDC</td></tr><tr><td>Input Impedance</td><td></td><td>2.4K Ohm</td><td></td></tr><tr><td>Operating Current Required</td><td>4 mA</td><td></td><td>60 mA</td></tr></table>		Input Voltage (DC)	MIN	NOM	MAX	Common Mode (Logic High) (Logic Low)	10 VDC -1 VDC	24 VDC 0 VDC	30 VDC 9 VDC	Common Mode Rejection			100 VDC	Input Impedance		2.4K Ohm		Operating Current Required	4 mA		60 mA
Input Voltage (DC)	MIN	NOM	MAX																		
Common Mode (Logic High) (Logic Low)	10 VDC -1 VDC	24 VDC 0 VDC	30 VDC 9 VDC																		
Common Mode Rejection			100 VDC																		
Input Impedance		2.4K Ohm																			
Operating Current Required	4 mA		60 mA																		
Digital Output Ratings	Output Voltage - 240 VAC Max. Output Current - 2.5 Amps Max. Form C relay contacts																				
Analog Input Ratings	Differential Input Voltage - $\pm 10$ VDC Max. Common Mode Input Voltage - 200 VDC Max. Common Mode Noise Rejection - 60 VDC Max. Accuracy - 0.25% F.S. Max. Drift - 0.12% F.S. Max.																				
Analog Output Ratings	Output Voltage - $\pm 10$ VDC Max. Output Current - 10 mADC Nom., 40 mADC Max. Common Mode Noise Rejection - 2 VDC Max. Drift - $\pm 1.2\%$ F.S. Max. Resolution - 0.025% F.S. Max. Accuracy - $\pm 1.8\%$ F.S. Max.																				

\* Additional Specifications are located in the supplemental drawing package.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

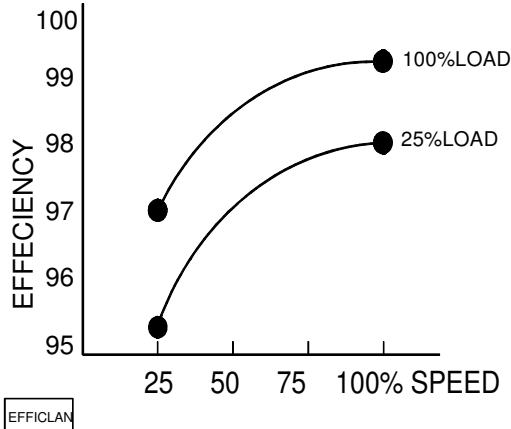
DESCRIPTION	SPECIFICATION*
Diagnostics	40 fault messages w/corrective action 12 front panel LED annunciators 16 event fault memory Signal Analyzer Sampling Rate - 90 Samples/Second Max., 110.8 Seconds/Sample Min. Recording Duration - 30.8 hours Max., 11 seconds Min.
RS485 Serial Link	Opto-isolated (Requires external 24V, 120 mA power supply), 120V common mode noise rejection
Pulse Generator Inputs: 2-Phase	1-30V peak-to-peak, 4700 ohm impedance, Transformer isolated, 120V common mode rejection, 0-20,200 Hz frequency range, 50% $\pm$ 20% duty cycle■
Buffered Pulse Generator Outputs: 2-Phase	5V @ 50mA, 0-25 KHz frequency range
Auxiliary Power Supplies	Digital I/O Supply Voltage Output = 24 VDC Nom., 26 VDC Max. Current Output = 80 mADC Max. Auxiliary AC Supply Voltage Output = 115 VAC Nom. Power Output = 50 VA Max. (units 56A and under) 100 VA Max. (units 110A and above) Serial Link Supply Voltage Output = 24 VDC Nom., 26 VDC Max. Current Output = 100 mADC Max. Safety Interlock Supply Voltage Output = 24 VDC Nom., 26 VDC Max. Current Output = 50 mADC Max. Pulse Generator Supply Voltage Output = 12 VDC Nom., 13.2 VDC Max. Current Output = 300 mA Max. (Short circuit proof) Pot Supplies Voltage Output = $\pm$ 10 VDC Max. Current Output = 5 mA Max.

\* Additional Specifications are located in the supplemental drawing package.

■ Consult Avtron regarding UNIPULSER™ information for additional duty cycle applications.



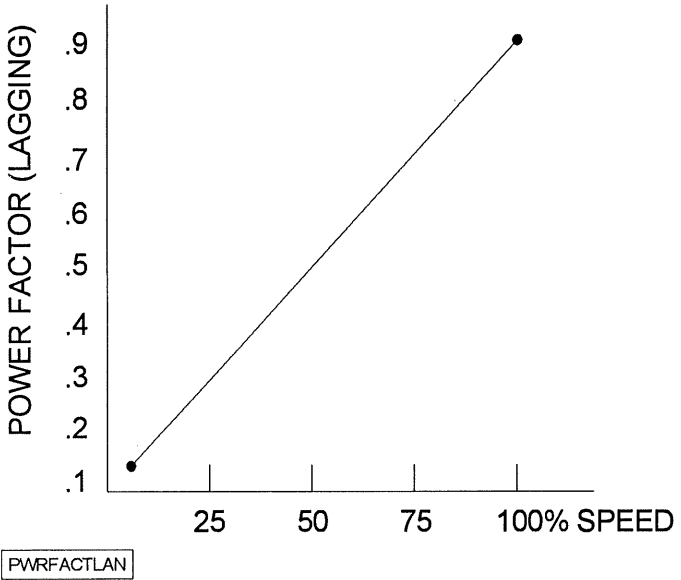
TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

DESCRIPTION	SPECIFICATION*																																		
Chassis Ambient Temperature - Enclosed (See outline drawing for minimum enclosure size.) - Open Chassis	0 to 40° C (32 to 104° F)  0 to 50° C (32 to 122° F) (50° C maximum surrounding air temperature rating)																																		
Storage Temperature***	-20 to 55° C (-4 to 131° F)																																		
Relative Humidity	95% non-condensing																																		
Operational Altitude	0 to 3,300 feet above sea level – no derating required. Above 3,300 feet – derated linearly by 1% per 300 ft.																																		
<p>Worst Case Power Loss</p> <table> <tr> <th>Drive P/N</th><th>Watts (approximate)</th></tr> <tr><td>DC0010</td><td>150</td></tr> <tr><td>DC0030</td><td>200</td></tr> <tr><td>DC0056</td><td>260</td></tr> <tr><td>DC0110</td><td>500</td></tr> <tr><td>DC0180</td><td>725</td></tr> <tr><td>DC0280</td><td>1000</td></tr> <tr><td>DC0360</td><td>1150</td></tr> <tr><td>DC0510</td><td>1400</td></tr> <tr><td>DC054X</td><td>1500</td></tr> <tr><td>DC055X</td><td>2050</td></tr> <tr><td>DC085X</td><td>2300</td></tr> <tr><td>DC155X-4</td><td>3900</td></tr> <tr><td>DC155X-B</td><td>4500</td></tr> <tr><td>DC250X</td><td>6100</td></tr> <tr><td>DC300X-A</td><td>7900</td></tr> <tr><td>DC300X-B</td><td>8300</td></tr> </table> <p>Power loss follows the approximate curve shown in Figure 1-17. Worst case power loss (total) is at 100% speed, 100% load. At other speeds and loads the percent loss is greater, but the total loss is less.</p>  <p>Figure 1-17. Efficiency vs. Speed</p>		Drive P/N	Watts (approximate)	DC0010	150	DC0030	200	DC0056	260	DC0110	500	DC0180	725	DC0280	1000	DC0360	1150	DC0510	1400	DC054X	1500	DC055X	2050	DC085X	2300	DC155X-4	3900	DC155X-B	4500	DC250X	6100	DC300X-A	7900	DC300X-B	8300
Drive P/N	Watts (approximate)																																		
DC0010	150																																		
DC0030	200																																		
DC0056	260																																		
DC0110	500																																		
DC0180	725																																		
DC0280	1000																																		
DC0360	1150																																		
DC0510	1400																																		
DC054X	1500																																		
DC055X	2050																																		
DC085X	2300																																		
DC155X-4	3900																																		
DC155X-B	4500																																		
DC250X	6100																																		
DC300X-A	7900																																		
DC300X-B	8300																																		

\* Additional Specifications are located in the supplemental drawing package.

\*\*\* A space heater may be necessary if condensation or excessive moisture is expected.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

DESCRIPTION	SPECIFICATION*
<p>Worst Case Power Loss (Continued)</p> <p>Power factor is highly dependent on operating speed. The curve in Figure 1-18 approximates power factor.</p>	 <p>Figure 1-18. Power Factor vs. Speed</p>

\* Additional Specifications are located in the supplemental drawing package.

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

## Bridge Interface Board

	DRIVE PART NUMBER			
	DC0010-0510 and 0550	DC0540, 0850-3000	DC0001 and DC0002 AFMs	DC0003, DC0004 and DC0005 AFMs
OUTPUT TO ARMATURE CIRCUIT	Outputs up to 12 SCR firing signals, 6 forward and 6 reverse. Contains pulse shaping circuitry.	Outputs up to 12 SCR firing signals, 6 forward and 6 reverse. Pulse shaping circuitry provided on armature bridge assembly.	Outputs up to 12 SCR firing signals, 6 forward and 6 reverse.	Outputs up to 24 SCR firing signals (12 forward, 12 reverse). Firing signal control is configurable through application specific software. Consult Avtron Industrial Automation, Inc., for information.
			SCR gate power supplied through internal 24 VDC supply.	Requires external pulse shaping circuitry for SCR firing (available from Avtron or others). Pulse shaping circuitry can be provided by an Avtron Gate Pulse Amplifier unit, P/N C23047. Consult Avtron Industrial Automation, Inc., for application specific information.
FIRING SIGNAL T.B.S	J3 and J7	J2 and J3	J2 and J3	J9 and J10
FIELD SUPPLY	See paragraph 1.2.6.	See paragraph 1.2.7.	See paragraph 1.2.7.	For DC0003 only: See paragraph 1.2.7. Also contains connection (J6) to support optional firing of an external single-phase field bridge.
ARMATURE CURRENT FEEDBACK	0.66V = 100% I <sub>arm</sub>	0.66V = 100% I <sub>arm</sub>	0.66V = 100% I <sub>arm</sub>	Selectable: DC0003 and DC0005: 0.666V = 100% or 5.00V = 100% DC0004: 0.666V = 100% or 3.33V = 100%

TABLE 1-1. ADDvantage-32 SPECIFICATIONS--Cont.

## Bridge Interface Board (Cont.)

	DRIVE PART NUMBER			
	DC0010-0510 and 0550	DC0540, 0850-3000	DC0001 and DC0002 AFMs	DC0003, DC0004 and DC0005 AFMs
ARMATURE VOLTAGE FEEDBACK	0 to 670 VAC	$\pm 10$ VDC Scaled by Avtron- supplied Voltage Isolation Board provided on armature bridge assembly.	$\pm 10$ VDC Requires customer- supplied external scaling circuit.	DC0003 and DC0005: $\pm 10$ VDC DC0004: $\pm 38.3$ VDC Requires customer- supplied external scaling circuit.
MISC.				The features below apply to DC0003 only: Auxiliary input is provided to accept $\pm 100$ mV input signal which is filtered (2 poles at 3.4mS) and amplified to $\pm 5.0$ VDC full scale and placed at an auxiliary output on J11.

## SECTION II

# KEYBOARD AND PARAMETER FUNCTIONS

\*\*\*\*\*

### WARNING

DO NOT OPERATE RADIO TRANSMITTERS or CELL PHONES IN THE VICINITY OF THE ADD-32. The ADD-32 is an electronic device. Although it is designed to operate reliably in typical industrial environments, the ADD-32 can be affected by radio and/or cell phone transmitters. It is possible to cause drive faults, inappropriate/unintended drive I/O activity, and unpredictable operation that could result in damage to the ADD-32, damage to other equipment, or serious injury to personnel.

Radio transmitter interference is a site specific phenomena. Generally, electrical wires connected to terminals on the ADD-32 are the conduits for radio interference. Interference can be minimized by good wiring design and installation practice. It is recommended that signs be posted in and around the drive system, warning of the possibility of interference if the drive is in operation. DO NOT USE radio transmitters or cell phones in the area.

Absence of a radio interference problem is no guarantee that a problem will never occur as conditions and environments can change.

\*\*\*\*\*

## 2.1

## KEY FUNCTIONS

Information generated by the ADDvantage-32 can be accessed using the alphanumeric keypad and LCD display located on the front of the chassis. The LCD display provides two rows of sixteen alphanumeric characters. Editing of displayed information is accomplished using the four keys located next to the LCD display. Keystroke functions are as follows:

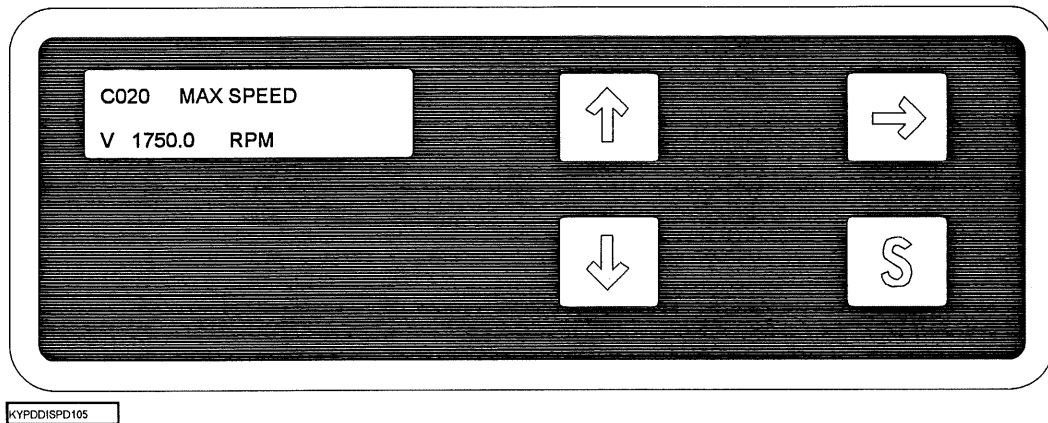






Figure 2-1. Keypad and Display

-  The up arrow key moves up through the loop of options in the menus, submenus, and parameters.
-  The down arrow key moves down through the loop of options in the menus, submenus, and parameters.
-  The right arrow key moves from menus to submenus to parameters.
-  The "S" key (S = select) moves from parameter to submenu to menu.

ADDKFUNCLAM

## 2.2 MENUS AND SUBMENUS

Information used in the ADDvantage-32 is organized into a menu format. Each menu contains either a submenu or a list of parameters. Similar values are organized together to simplify the location of information.

Figure 2-2 illustrates the menu format used. All information is set up in a loop format for easy access. Path flow through the menus is indicated by the arrows on the chart. Press the right arrow key to access the submenus and parameter values. Use the up and down arrow keys to scroll through the information. To return to the main menu, press the "S" key.

For example, the following sequence is used to view information in the FAULT FIFO menu.

1. Press the up or down arrow keys to scroll through the main menu options.
2. When FAULT FIFO appears on the display, press the right arrow key.
3. Scroll through the submenu options using the up and down arrow keys until the VIEW FAULT FIFO submenu appears.
4. Press the right arrow key to enter the VIEW FAULT FIFO submenu.
5. Press the up or down arrow keys to scroll through the parameter information.
6. Press the "S" key twice to return to the FAULT FIFO main menu.

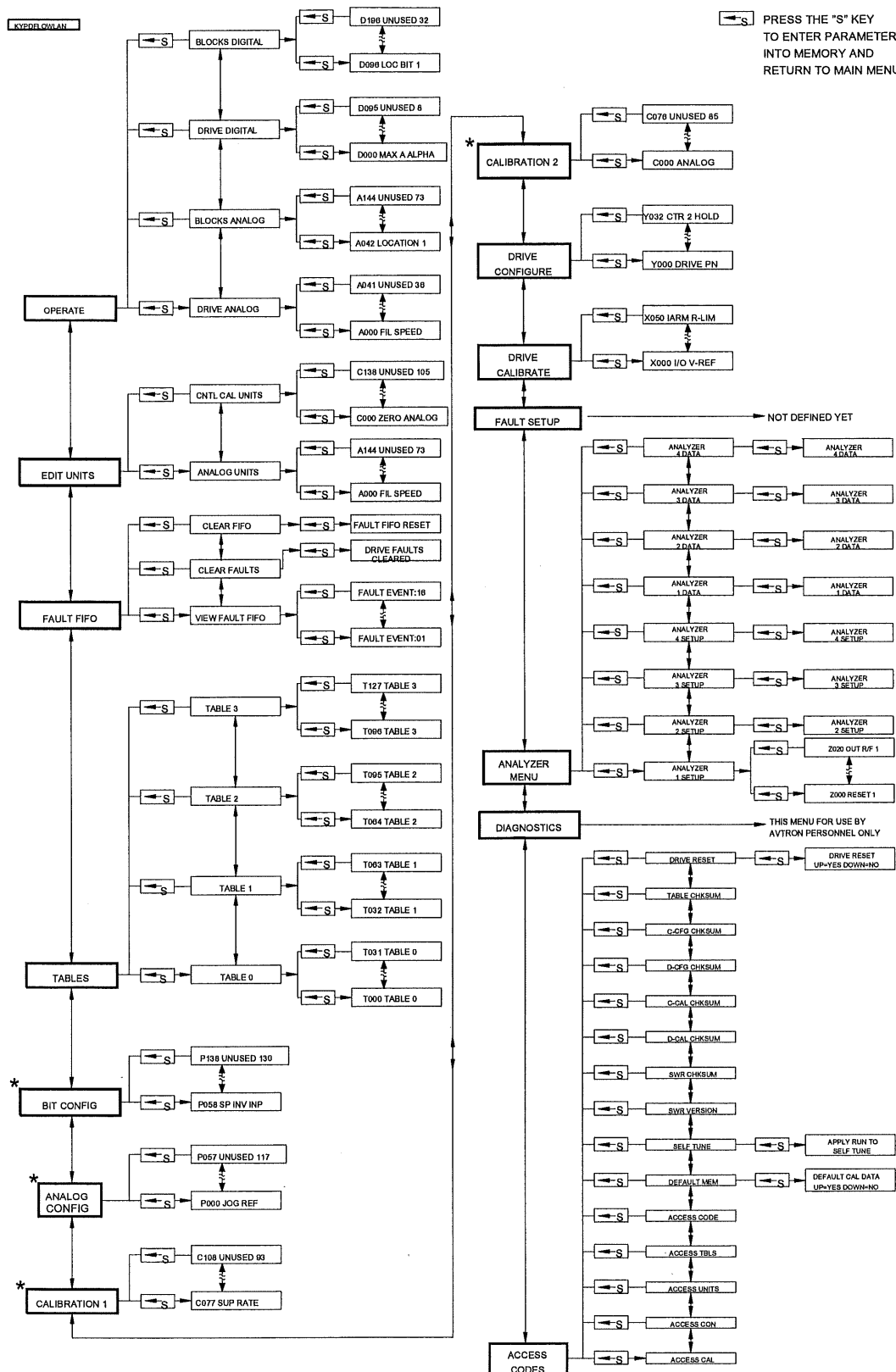


Figure 2-2. Keypad Flowchart

\*Name can be different based on application. See Appendix D for correct menu name for a particular parameter.



## 2.3 PARAMETER DEFINITION AND GROUPINGS

Parameters within the menus and submenus of the ADDvantage-32 are used to implement specific features in the application software.

There are several different types of parameters which are described as follows:

1. Calibration Parameters are numeric values entered for data such as limits, setpoints, or ramp rates.
2. Configuration Parameters are values used to select where information is going to come from or how specific features will function.
3. Analog Data is real time information contained in the ADDvantage-32 analog data table. This data is updated by the core software, application blocks, over the serial link/LAN, or the hardwired I/O.
4. Digital Data is real time information contained in the ADDvantage-32 digital data table. This data is updated by the core software, application blocks, over the serial link/LAN, or the hardwired I/O.

### 2.3.1 PARAMETER GROUPS

Parameters are defined by a four-digit code followed by a name or abbreviated description. The letter used as the first digit represents the particular group to which a parameter belongs. A typical parameter is shown as follows:

**P000:JOG REF**

Refer to Appendix C for specific parameter numbers and descriptions. Parameters are organized as shown in Table 2-1 and Figure 2-3.

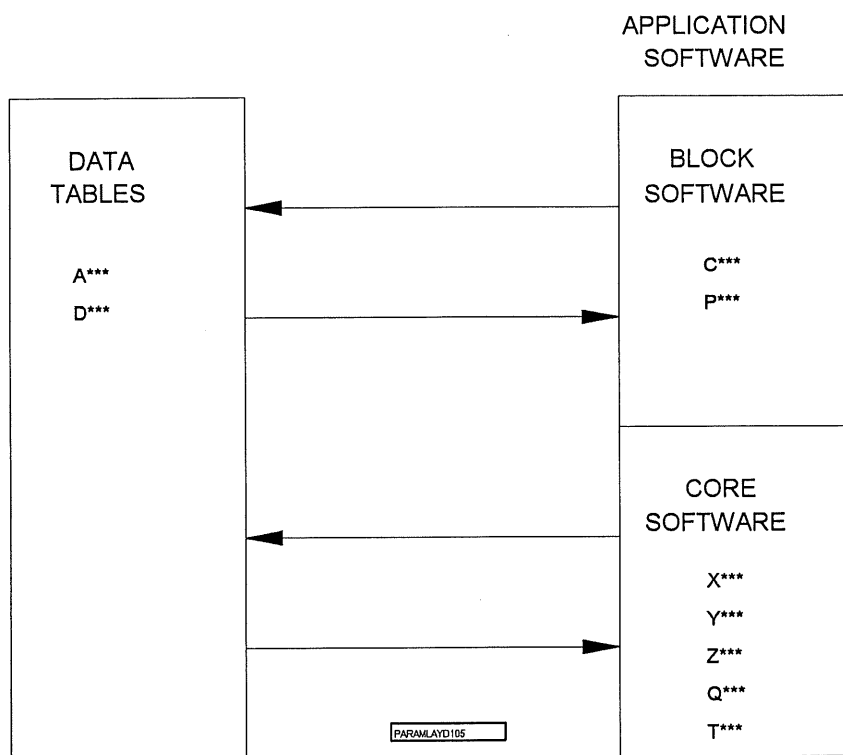


Figure 2-3. Parameter Layout

TABLE 2-1. PARAMETER ORGANIZATION

PARAMETER GROUP	PARAMETER TYPE	DESCRIPTION
X***	Calibration	X*** parameters calibrate the core software. Core parameters perform tasks specific to the ADDvantage-32 hardware being used.
Y***	Configuration	Y*** parameters configure the core software. These parameters set up the functionality of the ADDvantage-32 hardware.
C***	Calibration	C*** parameters calibrate the application block software being used. These parameters can be permanently fixed to specific blocks or can be configured using P*** parameters.
P***	Configuration	P*** parameters configure the application block software used with the ADDvantage-32. P*** parameters allow the option to link specific blocks together, or configure a C*** parameter to the input blocks.
A***	Analog Data	A*** parameters are real time floating point data. They represent all the information in the analog data table.
D***	Digital Data	D*** parameters are real time bit data. They represent all the values in the digital data table. A D*** parameter has a value of either one or zero. A one means the condition is true.
T***	Calibration Points	T*** parameters calibrate the data for the ADDvantage-32 function tables. The ADDvantage-32 has four function tables, each with 16 data points.
Z***	Calibration and Configuration	Z*** parameters are a mix of configurable and calibratable values used for the four built-in signal analyzers. See Section V.
Q***	Data Value	Q*** values are read-only parameters used by the Y*** and Z*** parameters. They represent selections available for certain parameters.
R***	LAN Auto Scan	R*** parameters configure the AUTO SCAN information to be accessed over the 802.4 LAN.

## 2.4

## NUMERIC TYPE PARAMETER FORMAT

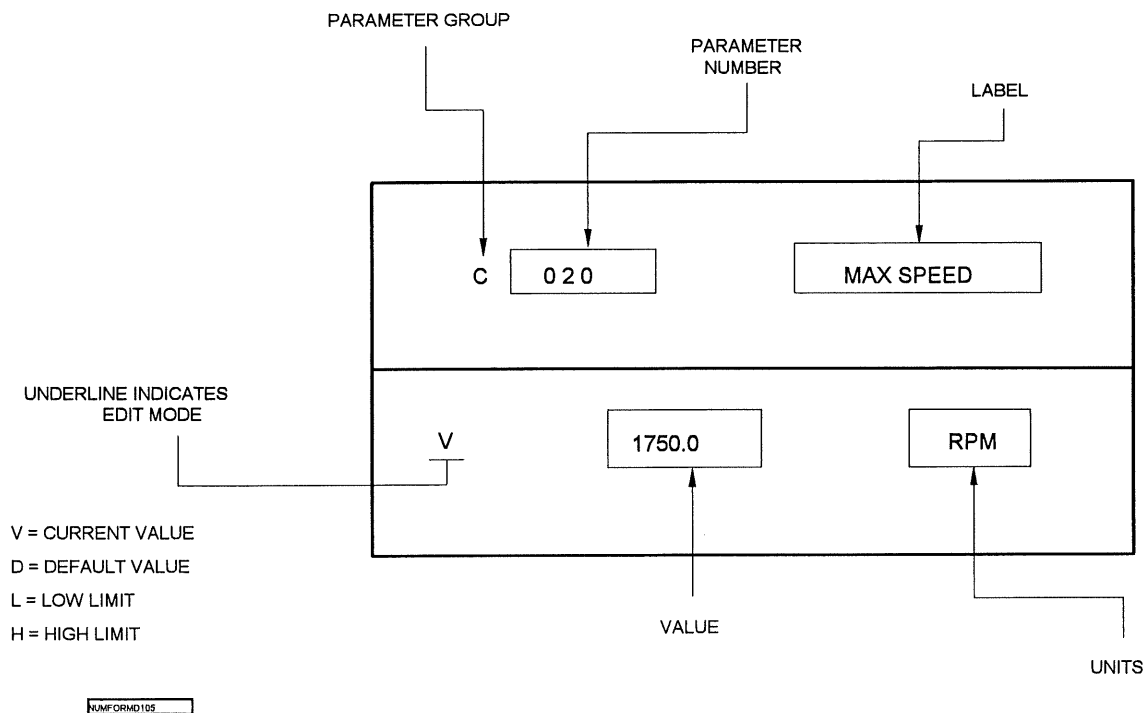


Figure 2-4. Numeric Format

1. Parameter Group - Represents the type of data to be edited. (See Table 2-1.)
2. Parameter Number - Each parameter within a data type has a unique parameter number. (See Appendix A.)
3. Label - Each parameter has a unique eleven character label. (See Appendix B.)
4. Bottom Left Character - Determines what type of value is displayed. The only value which can be edited is "V" which represents current value.
5. Value - Represents the value of a particular parameter to nine significant digits.
6. Units - Represents the value's units of measure. This text can be edited using the Edit Units menu.

## **2.5 EDITING A NUMERIC PARAMETER**

To edit a parameter, press the right arrow key. The bottom left most character will be underlined, indicating the location of the cursor. The cursor shows which character will be edited. Characters are edited one at a time.

### **NOTE**

If access to the parameter is locked out, the message "ACCESS DENIED" will be displayed. To allow entry to the edit mode, the proper parameter must be enabled in the ACCESS CODES menu.

1. Press the right arrow key until the cursor underlines the digit to be changed.
2. Press the up or down arrow key to display the possible choices.
3. When a choice is made, press the right arrow key to move the cursor or press the "S" key to enter the choice and exit the edit mode.

## 2.6

## CONFIGURATION TYPE PARAMETER FORMAT

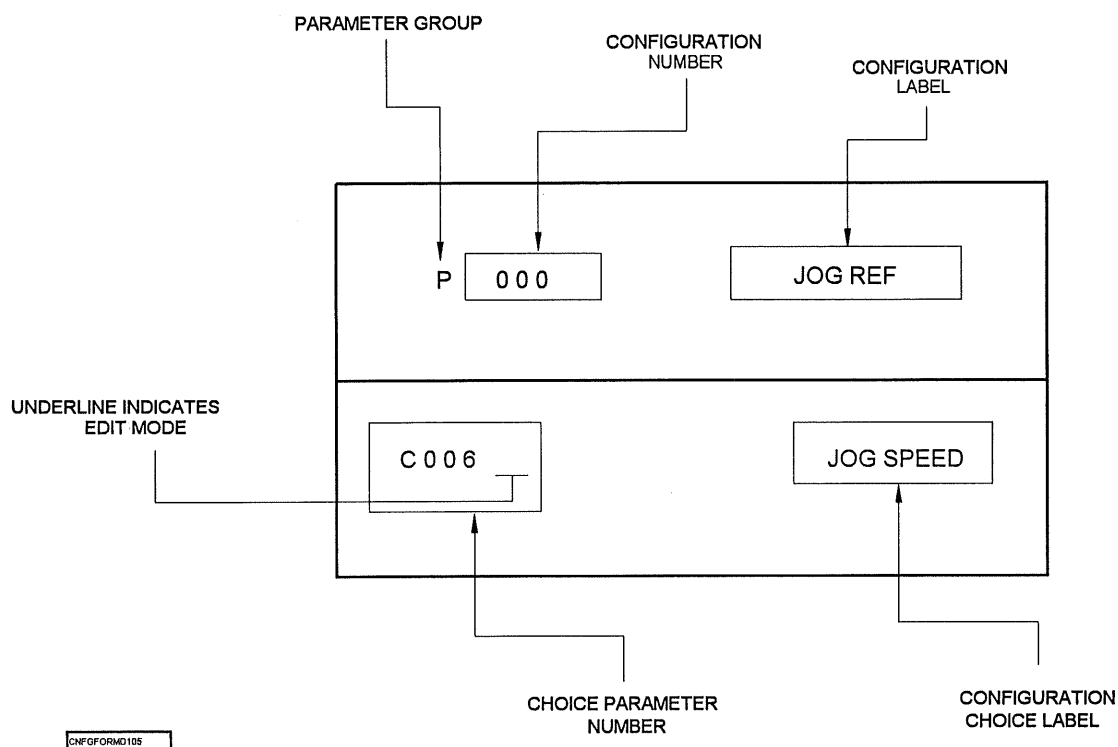


Figure 2-5. Configuration Format

1. Parameter Group - Represents the type of data to be edited. (See Table 2-1.)
2. Configuration Number - Each configuration parameter has a unique number. (See Appendix A.)
3. Configuration Label - Each configuration parameter has a unique label. (See Appendix B.)
4. Choice Parameter Number - Represents data type and number of the configuration choice.
5. Configuration Choice Label - Each configuration parameter has a unique eleven character label.

## 2.7

**EDITING A CONFIGURATION PARAMETER**

1. Press the right arrow key to enter the edit mode at the parameter to be changed. Verify that an underline, indicating location of the cursor, appears beneath the last number of the parameter ID number.
2. Press the up or down arrow keys to view the configuration choices.
3. Press the "S" key to store the new configuration and to exit the edit mode.

\*\*\*\*\*

**CAUTION**

**ALL "P" PARAMETER AND CERTAIN "Y" PARAMETER  
CHANGES WILL NOT BE IMPLEMENTED UNTIL  
POWER IS CYCLED OR THE DRIVE IS RESET, EXCEPT  
FOR THE LAN AUTOSCAN PARAMETERS.**

\*\*\*\*\*

The keypad flowchart in Figure 2-2 indicates with directional arrows the path to follow for viewing/editing software parameters. Table 2-2 provides descriptions of the various menus, submenus, and parameters.

TABLE 2-2. PARAMETER DESCRIPTION CHART

**NOTE:** The following table describes the menus and submenus available on the ADDvantage-32. Ranges shown for the parameters vary for each application software part number. They are provided for sample purposes only. Actual parameter names may vary. Refer to Appendix D provided with your specific nomenclature.

MAIN MENU   SUBMENU		DESCRIPTION	RANGE OF PARAMETERS
EDIT UNITS		Allows the user to change the units of measure of the parameter shown on the display. (i.e. Changing ACT SPEED units from FPM to RPM.)	
	CNTL CAL UNITS	Allows the user to change the units of measure for the calibration parameters.	C000 ZERO ANALOG   C124 TEN I GAIN
	ANALOG UNITS	Allows the user to change the units for the analog data parameters.	A000 FIL SPEED   A132 UNUSED 61
FAULT FIFO		From this menu, the user can reset the FAULT FIFO, view the FIFO, or reset the drive faults.	
	VIEW FAULT FIFO	The last sixteen events can be viewed from this submenu, last fault shown first. If ---- is displayed, FIFO has been cleared and is not filled with events.	FAULT EVENT:16   FAULT EVENT:1
	CLEAR FIFO	By pressing the right arrow key when in the submenu, the message FAULT FIFO RESET appears on display, erasing the events stored in the FIFO.	
	FAULT FIFO RESET	Message FAULT FIFO RESET appears for approximately two seconds, indicating that the fault FIFO is being cleared.	
	CLEAR FAULTS	By pressing the right arrow key, when in this submenu, the message DRIVE FAULTS CLEARED appears on the display. This will clear the present fault.	
	DRIVE FAULTS CLEARED	Message DRIVE FAULTS CLEARED appears for approximately two seconds, indicating that the current faults are being cleared.	



MAIN MENU   SUBMENU	DESCRIPTION	RANGE OF PARAMETERS
TABLES	Four tables are available to perform nonlinear functions such as square root. Sixteen data points are available to describe the function in each table. A table is implemented by executing the TABLE BLOCK. (See Section 4.)	
TABLE 0	First of four user available tables. Enter the sixteen X and Y data points for TABLE 0.	T000 TABLE 0 X0   T031 TABLE 0 Y15
TABLE 1	Second of four user available tables. Enter the sixteen X and Y data points for TABLE 1.	T032 TABLE 1 X0   T063 TABLE 1 Y15
TABLE 2	Third of four user available tables. Enter the sixteen X and Y data points for TABLE 2.	T064 TABLE 2 X0   T095 TABLE 2 Y15
TABLE 3	Fourth of four user available tables. Enter the sixteen X and Y data points for TABLE 3.	T096 TABLE 3 X0   T127 TABLE 3 Y15
BIT CONFIG *	All digital application configuration parameters can be viewed and edited. Drive must be reset to update edited values. (i.e. Configuring SUP ENABLE to USER 3 allows the third digital input to implement a speed slack step. )	P058 SP INV INP   P138 UNUSED 130
ANALOG CONFIG *	All analog application configuration parameters can be viewed and edited in this menu. Drive must be reset to update edited values. (i.e. Configuring SLACK UP to ANALOG IN 1 allows the first analog input to be the slack step value.)	P000 JOG REF   P057 UNUSED 117
CALIBRATION 1 *	First application calibration parameter menu. The parameters are broken down into different menus to reduce the size of the queues.	C077 SUP RATE   C108 UNUSED 93
CALIBRATION 2 *	Second application calibration parameter menu.	C000 ZERO ANALOG   C076 UNUSED 85
DRIVE CONFIGURE	Configuration parameters for drive setup can be viewed and edited in this menu. The drive does not need to be powered up again for the new value to be used. (i.e. Configure RUN INPUT to USER 1.)	Y000 DRIVE PN   Y032 CTR 2 HOLD

\*Name can be different based on application. See Appendix D for correct menu name for a particular parameter.

MAIN MENU   SUBMENU		DESCRIPTION	RANGE OF PARAMETERS
DRIVE CALIBRATE		Calibration parameters for drive setup and armature current loop tuning can be viewed and edited in this menu. (i.e. Scale the analog outputs.)	X000 I/O V REF   X050 IARM R-LIM
FAULT SETUP		Not defined yet.	
ANALYZER MENU		Allows user to set up, activate, and view the signal analyzer. There are setup and data submenus for each of the four analyzers.	
	ANALYZER 1 SETUP	Set up and activate signal analyzer 1. See Section V for operation of the Signal Analyzer.	Z000:RESET 1   Z020:OUT R/F 1
	ANALYZER 2 SETUP	Set up and activate signal analyzer 2. Similar to the configuration for channel #1. See Section V for operation of the Signal Analyzer.	Z100:RESET 2   Z120:OUT R/F 2
	ANALYZER 3 SETUP	Set up and activate signal analyzer 3. Similar to the configuration for channel #1. See Section V for operation of the Signal Analyzer.	Z200:RESET 3   Z220:OUT R/F 3
	ANALYZER 4 SETUP	Set up and activate signal analyzer 4. Similar to the configuration for channel #1. See Section V for operation of the Signal Analyzer.	Z300:RESET 4   Z320:OUT R/F 4
	ANALYZER 1 DATA	User can view data stored in analyzer. The bottom left character indicates the status of the analyzer as follows:  <div style="display: flex; justify-content: space-between;"> <div> U = Unused E = Enabled A = Armed and Enabled </div> <div> T = Triggered (gathering data) D = Done Collecting Data I = In Progress (outputting data) </div> </div> If the channel is done recording, the trigger event number and its value will be shown. Use the up/down arrow keys to view all 1000 events.	ANALYZER 1 DATA D500 100.01
	ANALYZER 2 DATA	User can view data stored in analyzer 2.	ANALYZER 2 DATA D500 100.01
	ANALYZER 3 DATA	User can view data stored in analyzer 3.	ANALYZER 3 DATA D500 100.01
	ANALYZER 4 DATA	User can view data stored in analyzer 4.	ANALYZER 4 DATA D500 100.01
DIAGNOSTICS		This menu for use for LAN diagnostics. See Section VIII for details.	

MAIN MENU SUBMENU	DESCRIPTION	RANGE OF PARAMETERS
ACCESS CODES	An access code is needed to allow entry into this menu. If the proper code is not entered, the message ACCESS DENIED will appear. User code 0.0 permits entry without a code. Code 216 allows entry into the menu at all times.	
ACCESS CAL	Allows modification of the calibration values.	Choices are NO, YES, and YES NONVOLATILE. If YES is selected it will default back to NO on the next drive powerup.
ACCESS CON	Allows modification of configuration parameters.	Choices are NO, YES, and YES NONVOLATILE. If YES is selected it will default back to NO on the next drive powerup.
ACCESS UNITS	Allows modification of parameter's units of measure such as Ft/Min of analog and calibration parameters.	Choices are NO, YES, and YES NONVOLATILE. If YES is selected it will default back to NO on the next drive powerup.
ACCESS TBLS	Allows modification of parameter values in the Tables menu.	Choices are NO, YES, and YES NONVOLATILE. If YES is selected it will default back to NO on the next drive powerup.
ACCESS CODE	Allows creation of a new access code for the main menu, which must be a 3-digit number. Access code 216 will always work with the user-defined code. Code may include decimal values along with 3-digit number.	Any number from 0-999 is valid.
DEFAULT MEM	Pressing the down arrow key (DOWN=NO) does not default the drive and returns to the submenu. Press the up arrow key (UP=YES) to default all drive calibration and configuration values. Record existing parameters prior to defaulting the drive or they will be lost. Drive will not default if run is energized, a warning will be issued if this occurs.	DEFAULT MEM UP=YES DWN=NO

MAIN MENU SUBMENU	DESCRIPTION	RANGE OF PARAMETERS
SELF TUNE	<p>To enable Self Tune, the following permissives must be met: bridge self test enabled, field disabled, and drive ESTOP picked up. Press the right arrow key to enable Self Tune. At that point, the drive run input will start Self Tune. To abort Self Tune at any time, remove the run or ESTOP input or press the S key.</p> <p style="text-align: center;"><b>CAUTION</b></p> <p>Lock the motor from rotation. If the motor starts to rotate, abort the Self Tune routines by pressing "S", Remove Run, or Remove ESTOP.</p> <p>When the Self Tune is completed, the drive will trip out on either a TUNE FAIL or TUNE PASS condition. Reset the fault to continue. The Self Tune finds the following drive calibration parameters:</p> <p style="text-align: center;">:I ARM CONTIN :ARM RESIST :Z-C CORRECT :I ARM PGAIN :IARM IGAIN</p>	SELF-TUNE PRESS "S" TO STOP
SWR VERSION	The first six numbers represent the Avtron software part number. The next two digits represent the version number of the software.	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">             69XXXXX   Software P/N           </div> <div style="text-align: center;">             XX   Version No.           </div> </div>
SWR CKSUM	This parameter represents the software checksum of the EEPROM integrated circuit. The drive checks the actual checksum to this value upon powerup to determine the integrity of the program.	
D-CAL CKSUM	This is the total sum of all drive calibration parameters. The purpose of this parameter is to determine if any of the parameters have been altered. Record this number after setup of the drive.	
C-CAL CKSUM	This is the sum of all application control calibration parameters. Record this number after setup of the drive.	
D-CFG CKSUM	This is the sum of all drive configuration parameters. Record this number after setup of the drive.	
C-CFG CKSUM	This is the sum of all application configuration parameters. Record this number after setup of the drive.	
TABLE CKSUM	This is the sum of all table data points. Record this number after setup of the drive.	
DRIVE RESET	Pressing the down arrow key (DOWN=NO) does not reset the drive but returns to the submenu. Press the up arrow key (UP=YES) to reset the drive. Drive will not reset if the run is energized; a warning will be issued if this occurs.	RESET DRIVE UP=YES DWN=NO

MAIN MENU   SUB MENU		DESCRIPTION	RANGE OF PARAMETERS
OPERATE		Display real time drive data	Default menu upon initial powerup:
	DRIVE ANALOG SUBMENU	Displays drive's real time analog data values such as line voltage, armature voltage and current, field voltage and current, I loop (CEMF, firing angles...)	A000 FIL SPEED   A041 UNUSED 36
	BLOCKS ANALOG SUBMENU	Displays all analog application data values generated and used in the software control blocks.	A042 LOCATION 1   A144 UNUSED 73
	DRIVE DIGITAL SUBMENU	Displays digital status bits not associated with software control blocks.	D000 MAX A ALPHA   D095 UNUSED 8
	BLOCKS DIGITAL SUBMENU	Displays all digital application data values generated and used in the software control blocks.	D096 LOC BIT 1   D196 UNUSED 32



## SECTION III

# CORE SOFTWARE OPERATION

The core software performs the following fundamental functions of the ADDvantage-32 hardware and software:

1. Hardware Setup and Diagnostics
2. I/O Configuration and Calibration
3. Input and Output Scanning
4. Individual Control Block Operation
5. Current Loop Operation
6. Four Channel Signal Analyzer Operation

This section describes the capabilities and functions of the core software and the X\*\*\*, Y\*\*\* parameters, as well as the corresponding A\*\*\* and D\*\*\* data table parameters. (The data table parameters are shown for reference purposes only and are not explained in detail unless required.) See Section V for the signal analyzer explanations.

### NOTE

Because parameter numbers vary according to software part number, specific parameter **numbers** are not shown. To locate a specific parameter number, refer to Appendix D.

## 3.1 DEDICATED INPUTS

Dedicated inputs are inputs located on the system board which perform a specific task. Each dedicated input is hard wired and operates independently of the application software, allowing failsafe operation even if a software problem occurs.

### 3.1.1 Emergency Stop (ESTOP)

When the ESTOP input is removed, the main contactor opens immediately and the gate firing is suppressed. Notice that the green EMERG STOP LED on the front of the ADDvantage-32 goes out.

After an ESTOP condition has occurred, the ESTOP and ESTOP RESET inputs must be applied to reset the ESTOP circuit. This illuminates the green EMERG STOP LED.

### 3.1.2 Emergency Stop Reset (ESTOP RESET)

A normally open pushbutton should be used for the ESTOP RESET. If the ESTOP input is present, then pressing the pushbutton resets the circuit. A reset must also be performed if a drive fault has occurred.

## 3.2 DEDICATED OUTPUTS

The following dedicated outputs are Form C contact outputs used for ADDvantage-32 status indication. Each output is hard wired and is not user programmable.

### 3.2.1 Drive O.K.

This Form C contact output signifies that there are no fault conditions in the ADDvantage-32. If a critical fault occurs, this output contact opens and remains open until the fault is cleared.

### 3.2.2 Motor Auxiliary Contactor

This Form C contact output opens if the main contactor is open, or closes if the main contactor is closed.

## 3.3 CONFIGURABLE DIGITAL INPUTS

### D\*\*\* Parameters

D\*\*\*:USER 1  
thru  
D\*\*\*:USER 14

The 24 VDC digital inputs are represented by a value in the digital data table. Each input is scanned by the core software to determine if it is in an ON or OFF state. Once this state is determined, the corresponding D\*\*\*:USER X parameter is set in the digital data table. This bit can then be used by other areas of the application software to enable specific functions.

Six digital inputs are located on the maxi system board and are represented by parameters D\*\*\*:USER 1 thru D\*\*\*:USER 6. Eight more inputs are available by adding the FAX-32 board. These inputs are represented by D\*\*\*:USER 7 thru D\*\*\*:USER 14 in the digital



data table. If the FAX-32 board is not used, the values for the additional eight parameters are always OFF.

### 3.4 CONFIGURABLE DIGITAL OUTPUTS

#### Y\*\*\* Parameters

Y\*\*\*:USER LED PT  
Y\*\*\*:DIG OUT 1  
Y\*\*\*:DIG OUT 2  
Y\*\*\*:DIG OUT 3  
Y\*\*\*:DIG OUT 4

The digital outputs are Form C contact outputs located on the System Board. Each output is configurable to a value in the digital data table. If the value in the data tables is ON, the output is ON. When the data table value is OFF, the output is OFF. Outputs are always functional and can be disabled by configuring them to either D\*\*\*:ZERO BIT or D\*\*\*:ONE BIT, which holds the output in a constant state.

For example, if a particular application requires that a contact output be closed when a fault occurs, perform the following:

1. Locate the value in the digital data table which signifies an ADDvantage-32 fault. (D\*\*\*:FAULT)
2. Configure Y\*\*\*:DIG OUT 1 to D\*\*\*:FAULT. Any time a fault occurs, the first digital output closes.

The user LED is similar in that it is configured to a digital data bit. When the bit goes high, the LED will light. The user LED is the first yellow LED on the drive.

### 3.5 LOGIC SEQUENCE

#### Y\*\*\* Parameters

Y\*\*\*:RUN INPUT  
Y\*\*\*:JOG INPUT  
Y\*\*\*:THRD INPUT  
Y\*\*\*:CLR FLT INP  
Y\*\*\*:ILIM HI INP  
Y\*\*\*:ILIM LO INP  
Y\*\*\*:MC CLOSE

#### D\*\*\* Parameters

D\*\*\*:IOC PT  
D\*\*\*:ESTOP IN  
D\*\*\*:FWD BR ACT  
D\*\*\*:REV BR ACT  
D\*\*\*:FLD LOSS PT  
D\*\*\*:SPD MIN PT  
D\*\*\*:FLD ECON PT

Y\*\*\* Parameters

Y\*\*\*:MC CLS ENA  
Y\*\*\*:FLD CNTL  
Y\*\*\*:FLD V-CMD  
Y\*\*\*:USR LED PT  
Y\*\*\*:F-FIFO CLR  
Y\*\*\*:F-CLR ON M

D\*\*\* Parameters

D\*\*\*:M TIMER PT  
D\*\*\*:PLL LOCK PT  
D\*\*\*:ARM ENABLE  
D\*\*\*:FLD ENABLE  
D\*\*\*:DOK OUT  
D\*\*\*:M CONTACTOR  
D\*\*\*:USER LED  
D\*\*\*:I-LIM LED  
D\*\*\*:FWD BR LED  
D\*\*\*:REV BR LED  
D\*\*\*:DFAULT LED  
D\*\*\*:F-LOSS LED  
D\*\*\*:IOC LED  
D\*\*\*:RUN LED  
D\*\*\*:RUN ENABLE  
D\*\*\*:JOG ENABLE  
D\*\*\*:THRD ENABLE  
D\*\*\*:FAULT  
D\*\*\*:RUNX  
D\*\*\*:RUN REQUEST  
D\*\*\*:MAX IARM  
D\*\*\*:MIN IARM  
D\*\*\*:CNTL INHIB  
D\*\*\*:USER 1  
D\*\*\*:USER 2  
D\*\*\*:USER 3  
D\*\*\*:USER 4  
D\*\*\*:USER 5  
D\*\*\*:USER 6  
D\*\*\*:NOT USER 1  
D\*\*\*:NOT USER 2  
D\*\*\*:NOT USER 3  
D\*\*\*:NOT USER 4  
D\*\*\*:NOT USER 5  
D\*\*\*:NOT USER 6  
D\*\*\*:IARM MIN PT  
D\*\*\*:IA MIN DELY  
D\*\*\*:SCR ENABLE  
D\*\*\*:IA SEAL  
D\*\*\*:REV\_LOCKOUT  
D\*\*\*:ONE BIT  
D\*\*\*:ZERO BIT

## 3.6

## DRIVE SEQUENCE RUNG DESCRIPTIONS

Figure 3-1 (on the following 15 pages) is a ladder logic diagram of the internal interlocks for the core software. These rungs determine when specific features are enabled and disabled. D\*\*\* parameters listed are values found in the digital data table. See Section II and Appendix C for parameter explanations. Figure 3-1 applies only to AC to DC Converter software part number 692XXX or 694XXX.

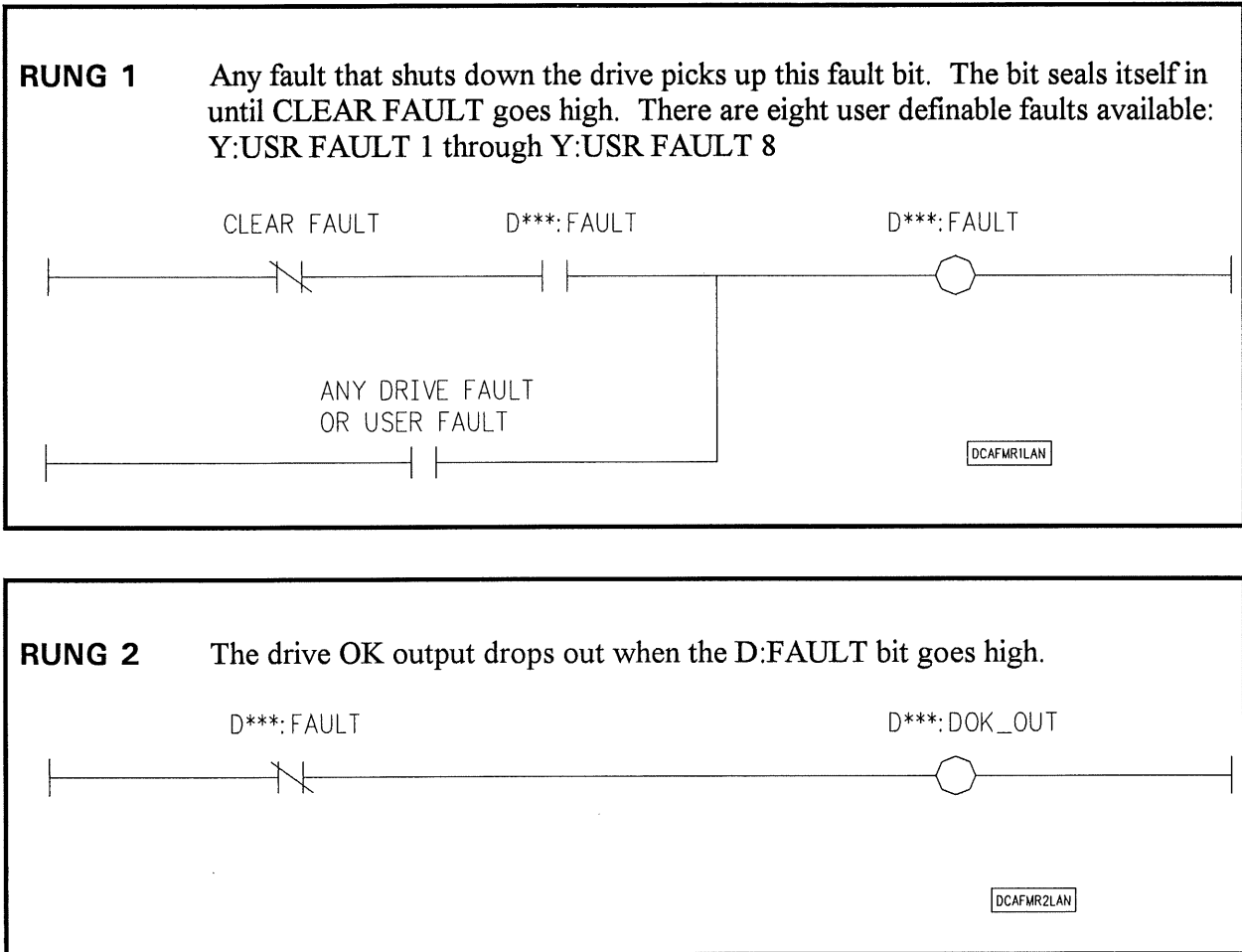


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 1 of 14)

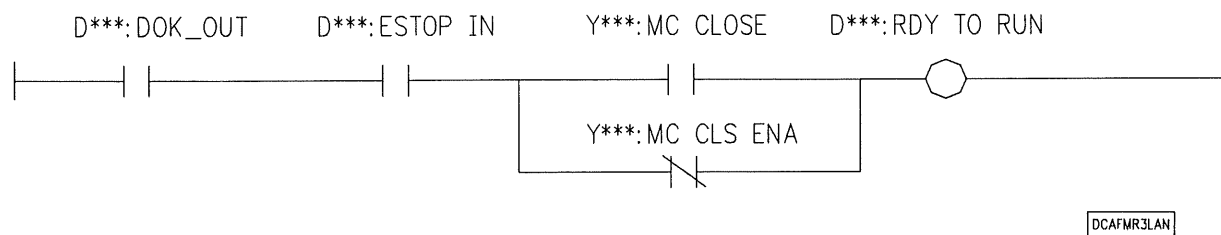
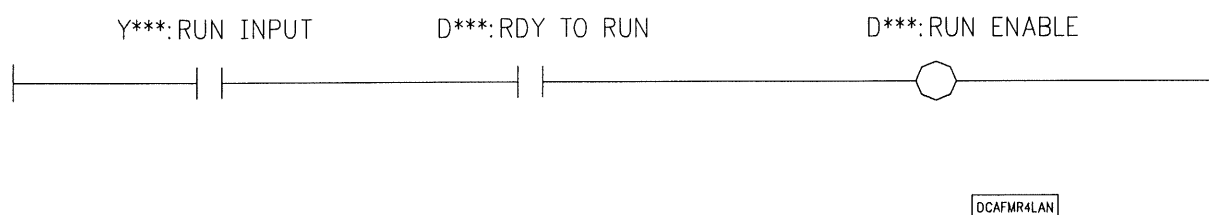
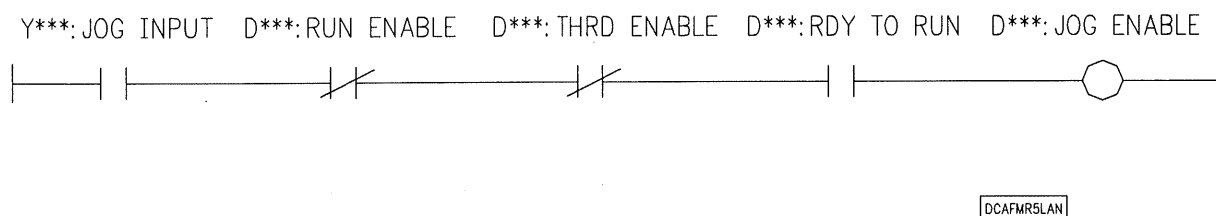
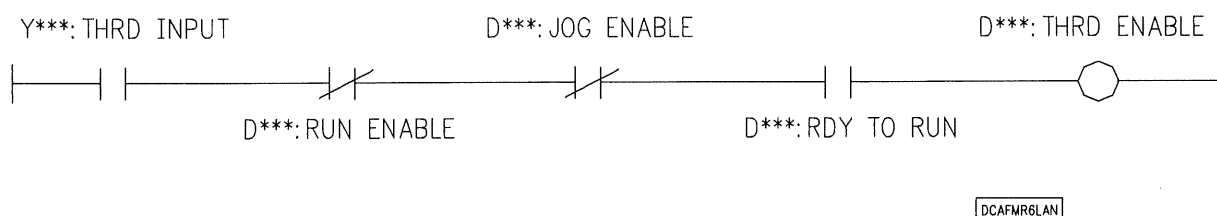
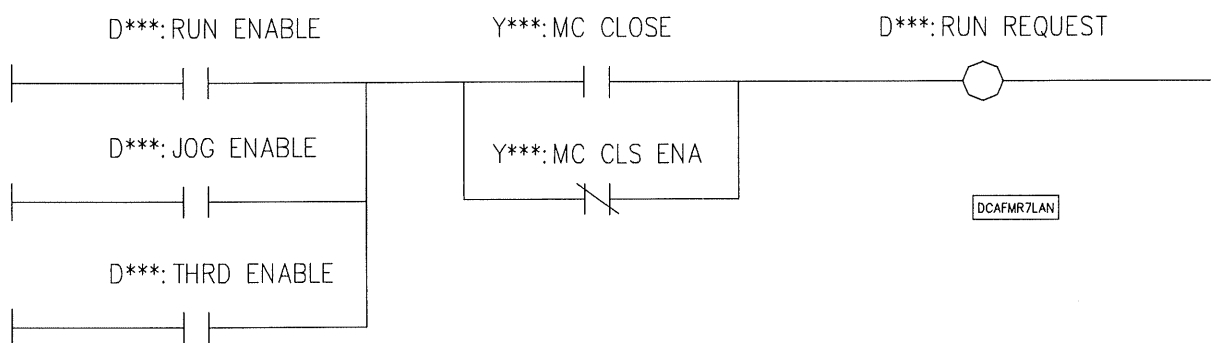
**RUNG 3** Ready for a run, jog or thread.**RUNG 4** This bit picks up the drive motor contactor and enables the run reference to the speed loop.**RUNG 5** This bit picks up the drive motor contactor and enables the jog reference to the speed loop.

Figure 3-1. ADDvantage-32 Logic Diagram (sheet 2 of 14)

**RUNG 6** This bit picks up the drive motor contactor and enables the thread reference to the speed loop.



**RUNG 7** A run, jog, or thread command is requested. If the drive is set up for an external signal to pick up the motor contactor, it must be closed before the D:RUN REQUEST will go high.



**RUNG 8** D:RUNX picked up on a run, jog, or thread command is requested. It stays in until the D:SPD MIN PT goes high or there is a fault or ESTOP. If you want the contactor to open immediately after run removal, configure D:SPD MIN PT to D:ONE BIT else set it equal to D:AT ZERO SPD.

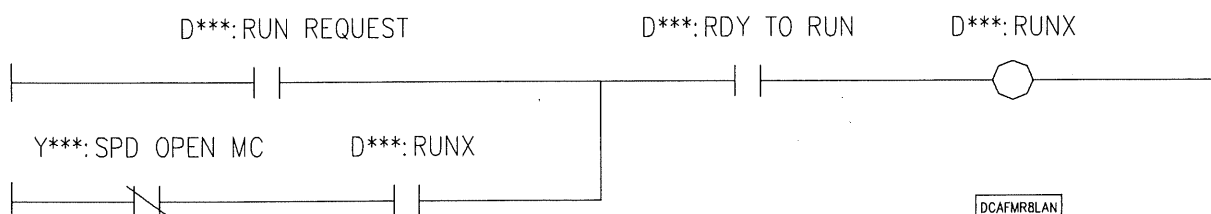
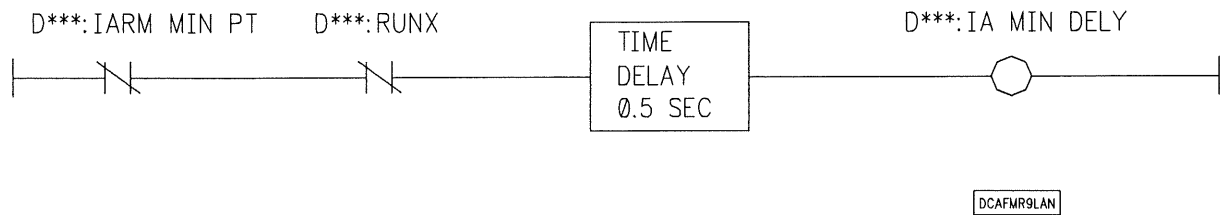
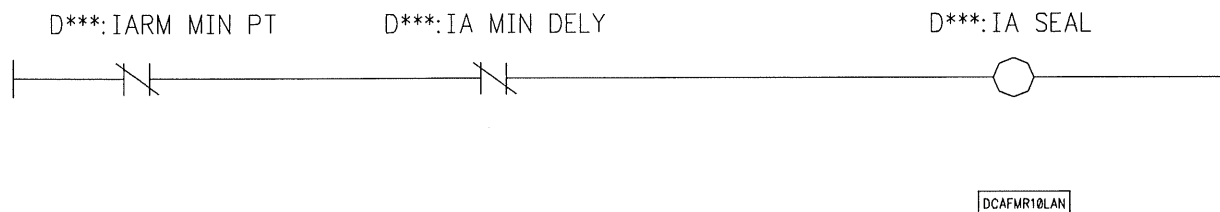


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 3 of 14)

**RUNG 9** Delay to hold in the motor contactor and SCR enable until armature current reaches near zero. It allows a delay of up to half a second.



**RUNG 10** This sets the seal-in bit to keep the motor contactor in and the SCR's enabled until the armature current reaches near zero or a half second after the contactor is commanded open.



**RUNG 11** This is a time delay of 60 seconds after the motor contactor is commanded open. (Used for the field economy bit.)

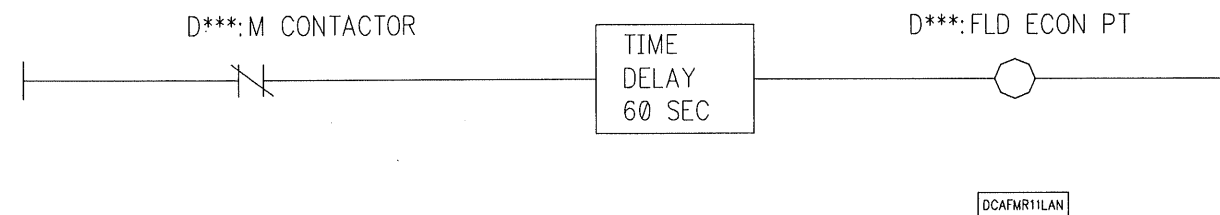
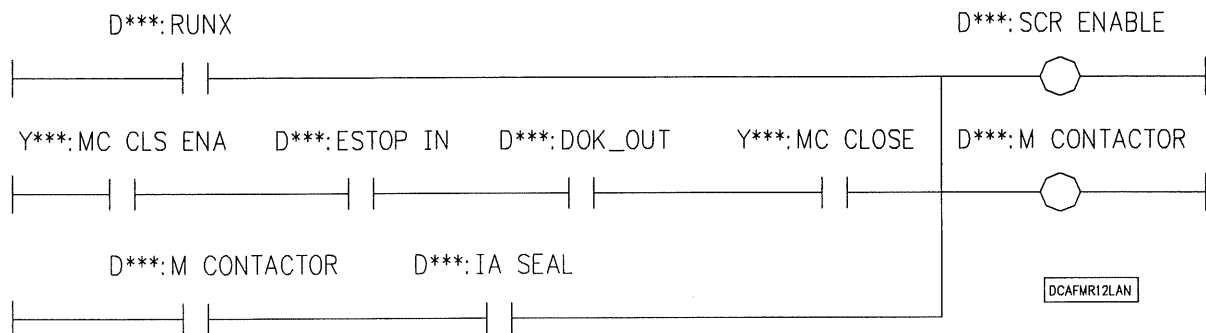


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 4 of 14)

**RUNG 12** Commands the motor contactor to close and enables the gate power to the SCR's. This can be done automatically when RUNX is applied or by an external motor contactor close command configured to Y:MC CLOSE. The output is held in until armature current reaches near zero or after a half second after commanded open. This is to prevent inverting faults.



**RUNG 13** This delays D:ARM ENABLE until the motor contactor has a chance to pick up. The delay is based on drive size from 150 ms on a 10 amp drive to 500 ms on a 510 and 550 amp drive and 750 ms on AFM's. The parameter X\*\*\*:MC DLY ADJT can adjust the delay, more or less by entering a positive or negative number respectively. X\*\*\* can be entered in "ticks," based on line frequency (2.777 ms on 60 Hz). Software will not allow delays less than 27 ms.

**WARNING:** Incorrect setting of the parameter can result in bridge self test failures or IOC's on application of runs to the drive. Also, the value SHOULD NOT be changed if there is any intention of applying the ADD-32 to an already spinning motor.

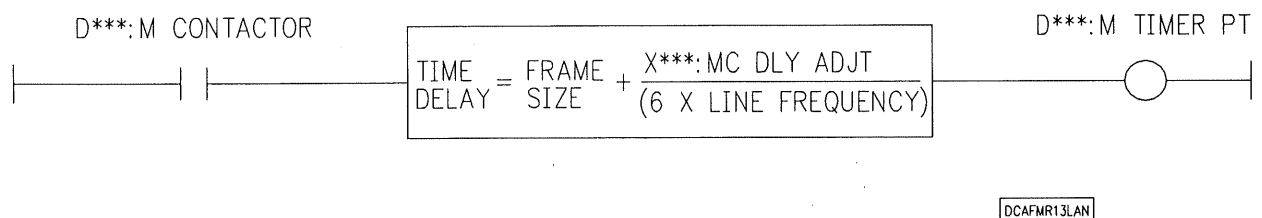
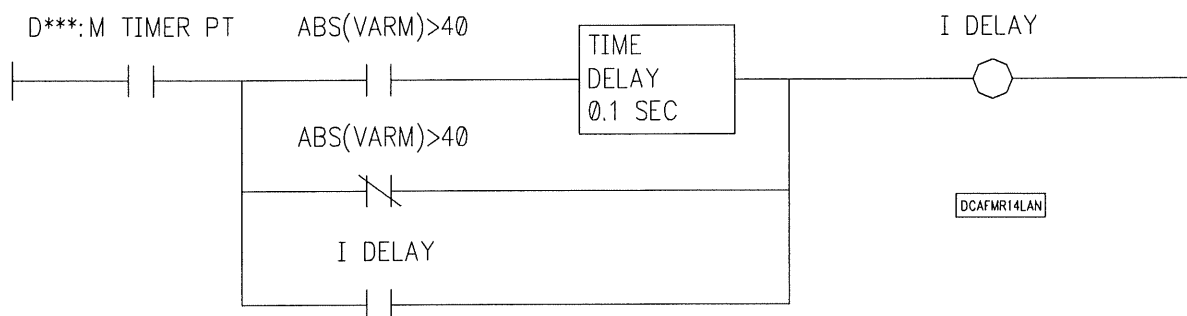
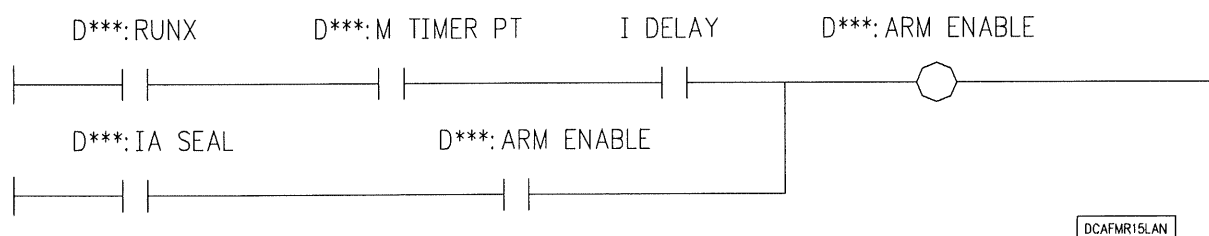


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 5 of 14)

**RUNG 14** This delay is to sense if there is actual CEMF on the motor when the contactor is closed. The delay is added to allow an accurate reading of motor CEMF in the event of a drive starting into a spinning motor.



**RUNG 15** D:ARM ENABLE allows the SCR's to fire and is used in the application portion of the software to release integrators and ramps.



**RUNG 16** Delay to check if the gate power has been removed two seconds after the contactor is commanded open.

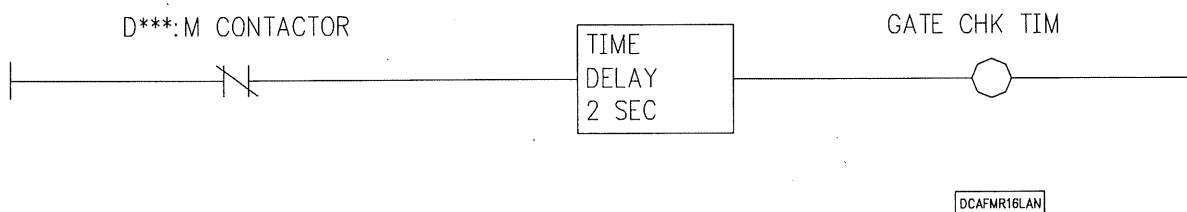
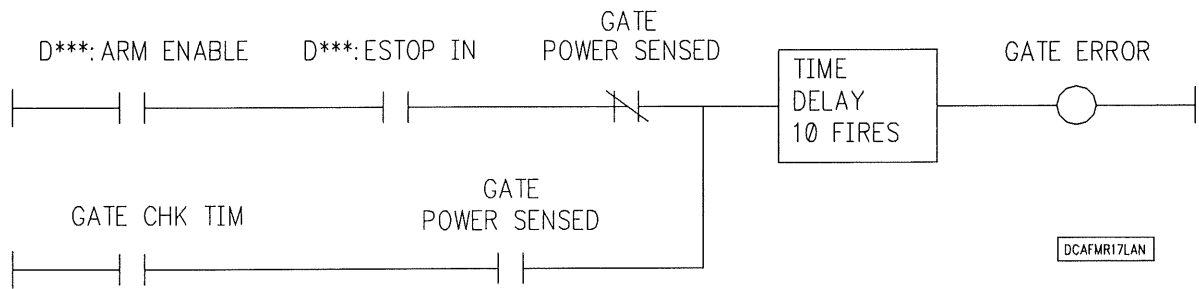


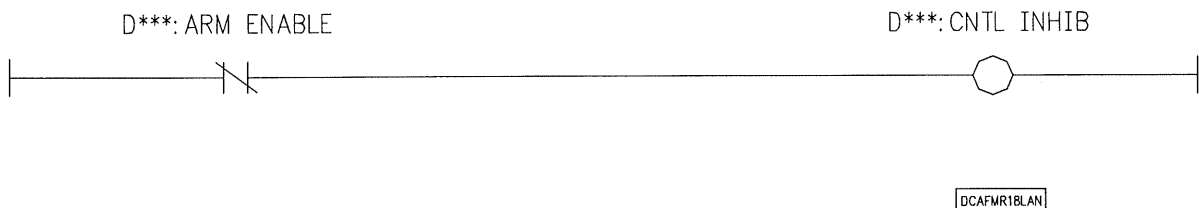
Figure 3-1. ADDvantage-32 Logic Diagram (sheet 6 of 14)



**RUNG 17** Gate error fault if the state of the sense signal is wrong for ten SCR firings. If the contactor is opened for two seconds, the gate power should be off. If D:ARM ENABLE is high, the gate power should be present already.



**RUNG 18** D:CNTRL INHIB is the opposite of D:ARM ENABLE. It is used in the application software to preset integrators and hold ramps.



**RUNG 19** The motor field can be enabled, disabled, or switched on or off by a digital bit. If the field is commanded, then it stays picked up until D:ARM ENABLE drops out. Field loss is enabled whenever D:FLD ENABLE is high or if Y:FIELD CNTL is set to digital bit.

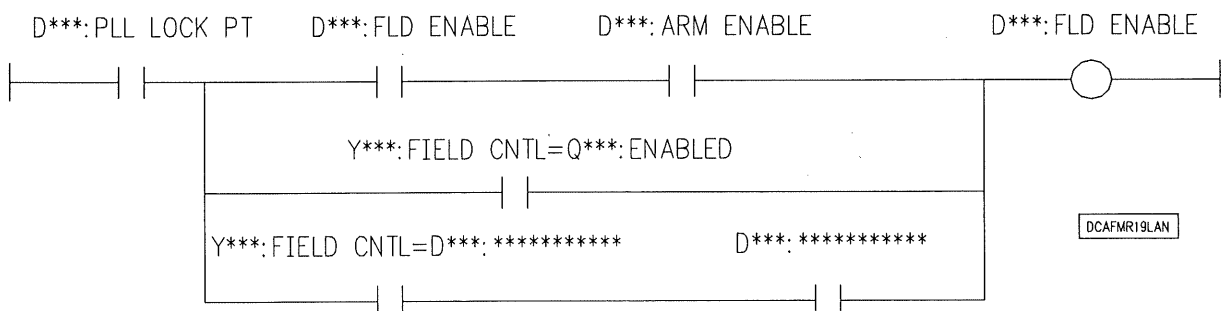
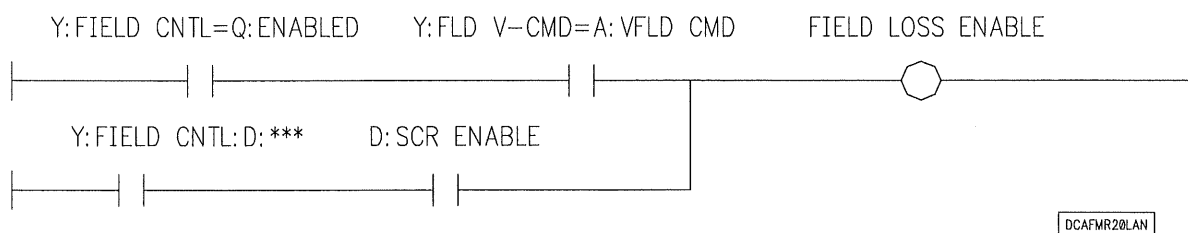


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 7 of 14)

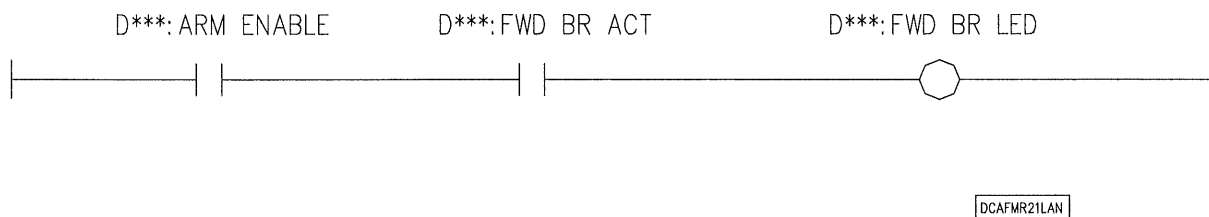
**RUNG 20** Field loss protection is enabled in the following two sequences:

If Y:FIELD CNTL is set to Q:ENABLED and the field voltage reference Y:FLD V\_CMD is configured to the output of the field current loop A:VFLD CMD.

If Y:FIELD CNTL is set to a digital bit, then field loss is enabled at any time the armature SCR's are enabled.



**RUNG 21** Lights the amber forward bridge LED.



**RUNG 22** Lights the amber reverse bridge LED.

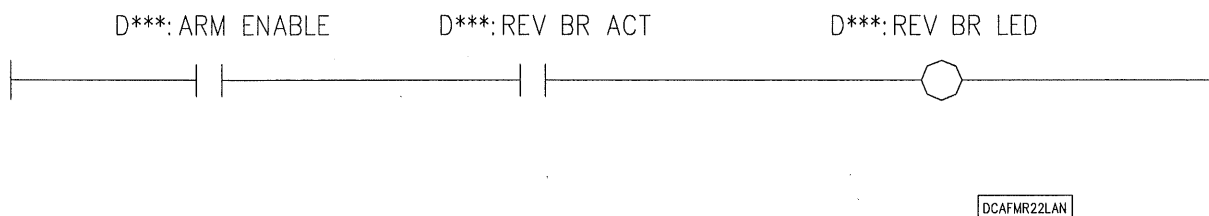


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 8 of 14)

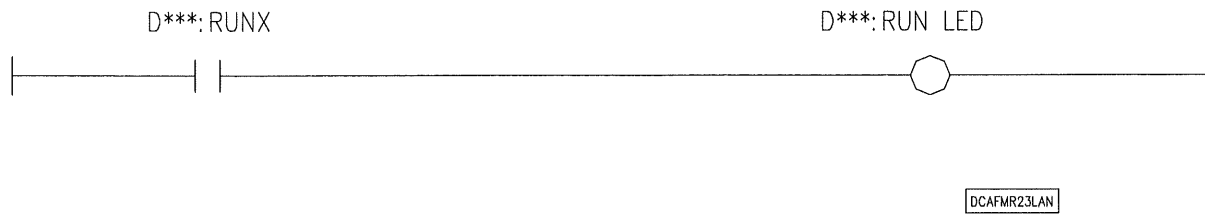
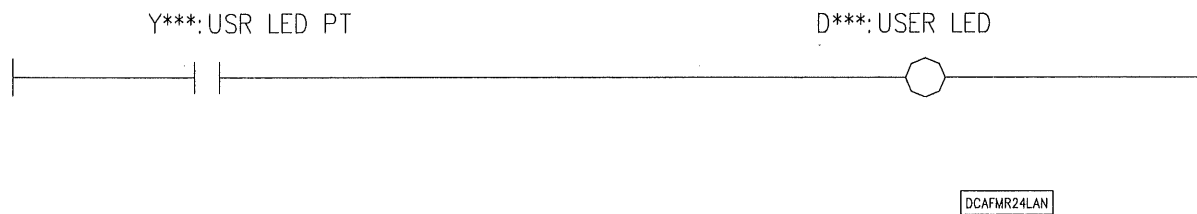
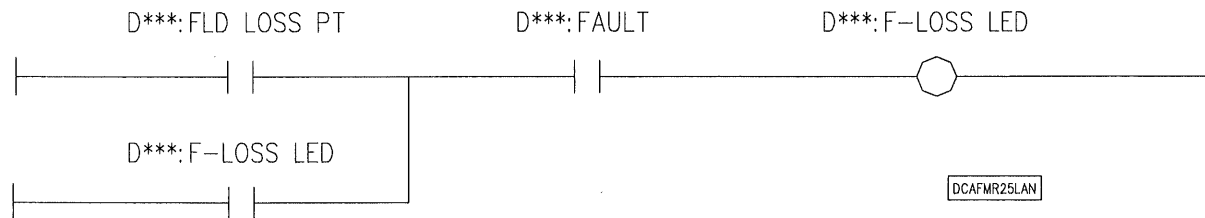
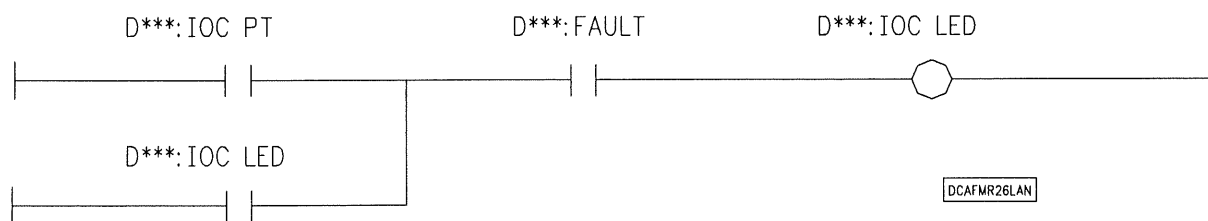
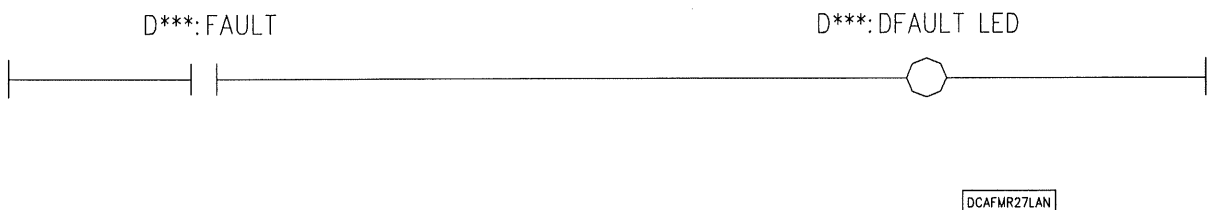
**RUNG 23** Lights the green running LED.**RUNG 24** Lights the amber user defined LED.**RUNG 25** Lights the red field loss LED and seals it in until the faults are cleared.

Figure 3-1. ADDvantage-32 Logic Diagram (sheet 9 of 14)

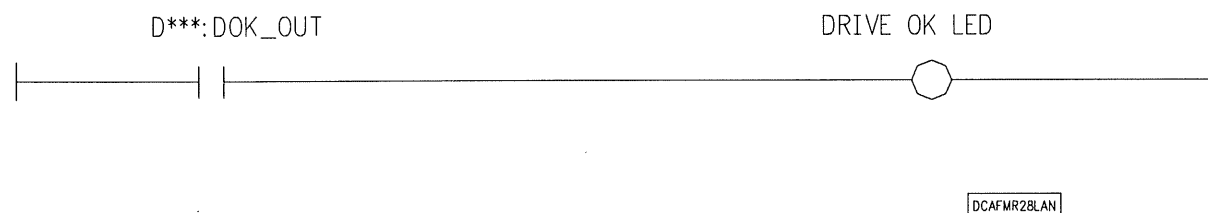
**RUNG 26** Lights the red instantaneous overcurrent LED and seals it in until the faults are cleared.



**RUNG 27** Lights the red drive fault LED.



**RUNG 28** Lights the green Drive OK LED.



**RUNG 29** Lights the green ESTOP OK LED.

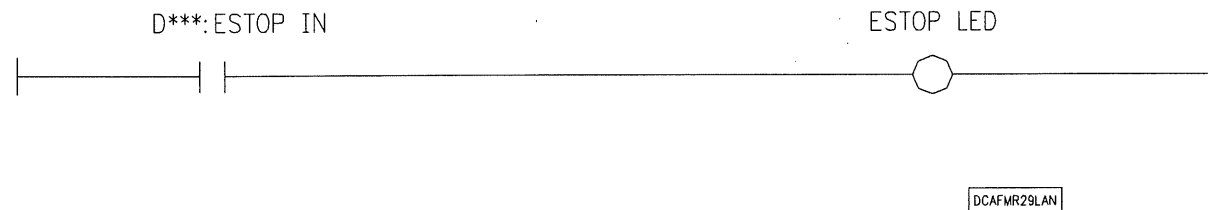
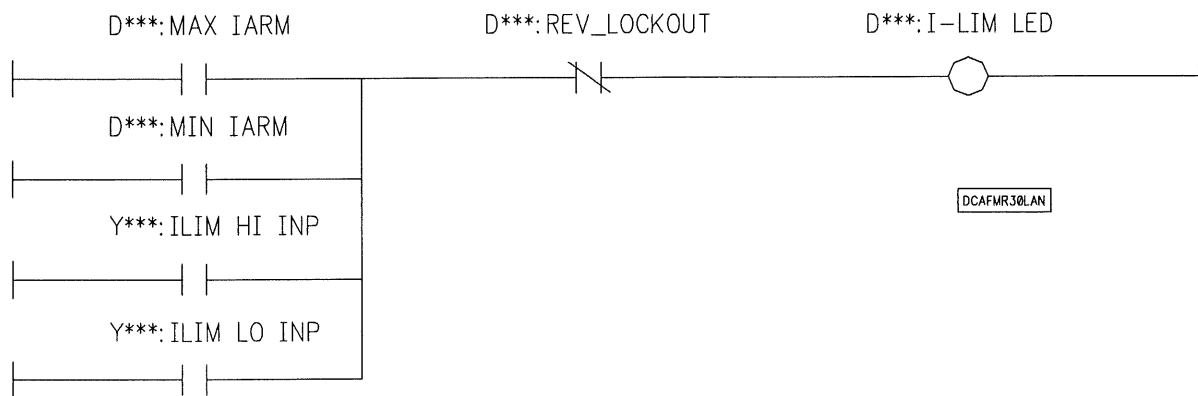


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 10 of 14)

**RUNG 30** Lights the amber current limit LED. To properly light the LED, the Y parameters must be set to the in-limit conditions of the speed loop PI regulator.



**RUNG 31** The fault FIFO can be cleared from the keyboard or from a digital bit configured to Y:F-FIFO CLR.

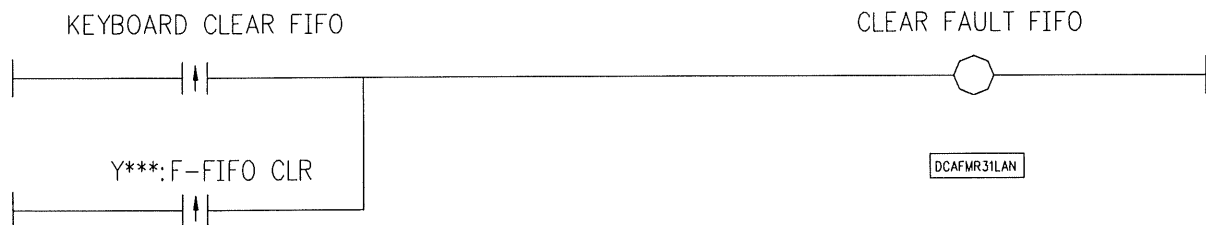
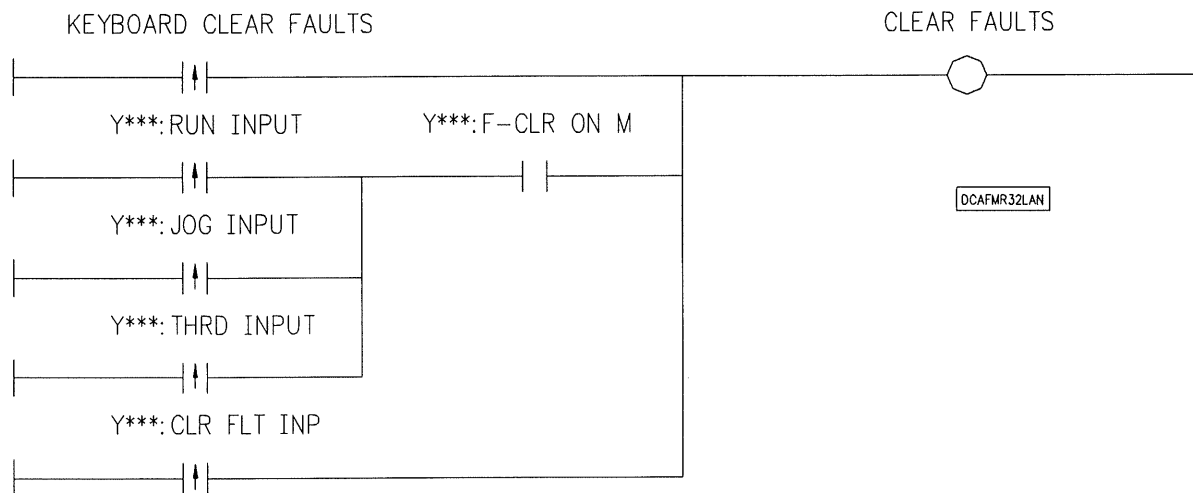
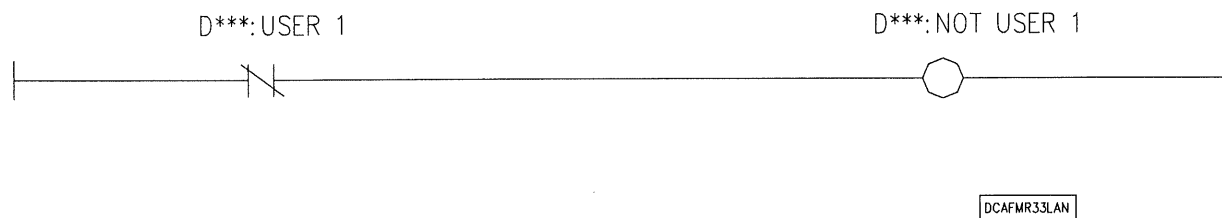


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 11 of 14)

**RUNG 32** A drive fault can be cleared by the keyboard, digital bit configured to Y:CLR FLT INP or on the next run, jog, or thread command if Y:F-CLR ON M is enabled. Faults will also be cleared on a repower of the drive.



**RUNG 33** D:NOT USER 1 is the inverse of the digital input D:USER 1.



**RUNG 34** D:NOT USER 2 is the inverse of the digital input D:USER 2.

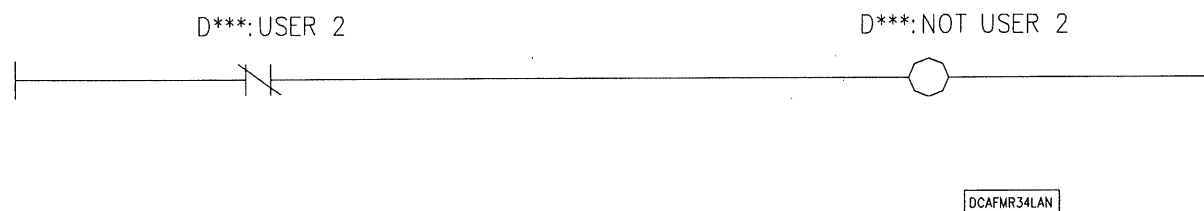
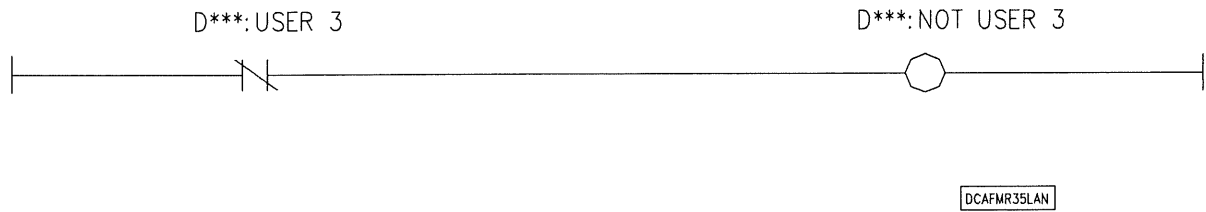
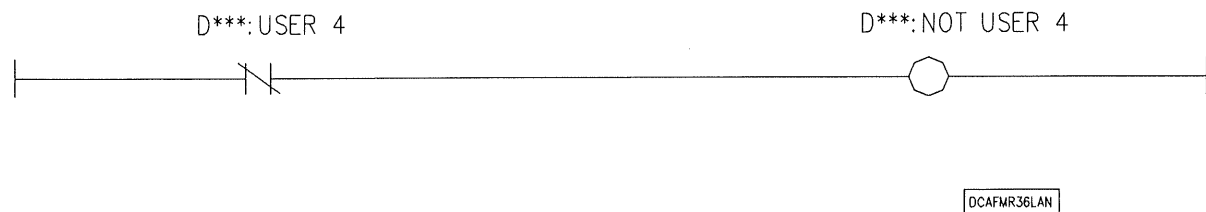


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 12 of 14)

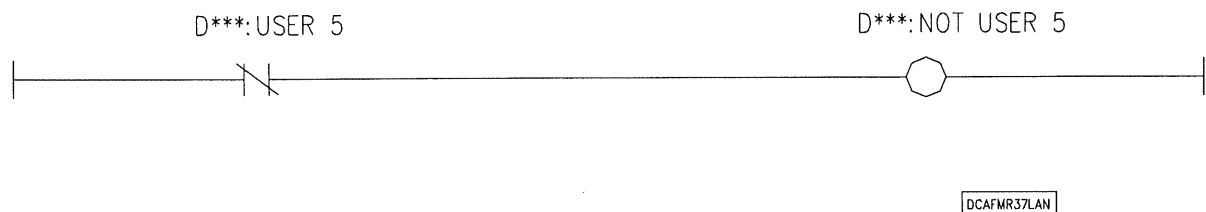
**RUNG 35** D:NOT USER 3 is the inverse of the digital input D:USER 3.



**RUNG 36** D:NOT USER 4 is the inverse of the digital input D:USER 4.



**RUNG 37** D:NOT USER 5 is the inverse of the digital input D:USER 5.



**RUNG 38** D:NOT USER 6 is the inverse of the digital input D:USER 6.

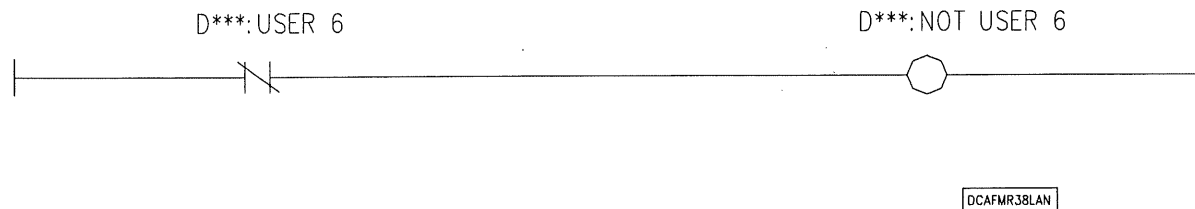
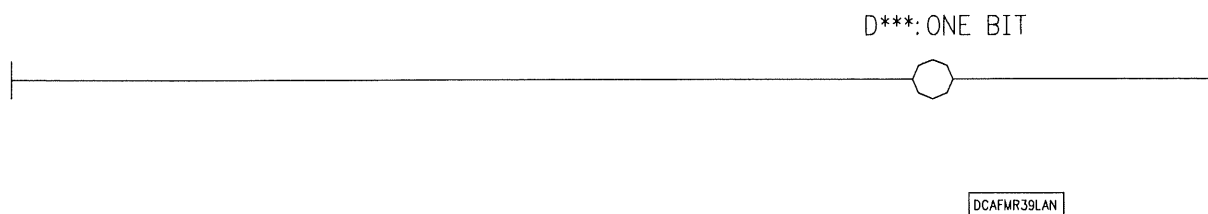


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 13 of 14)

**RUNG 39** D:ONE BIT is always high. Applications blocks can use this to always enable a function.



**RUNG 40** D:ZERO BIT is always low. Application blocks can use this to always disable a function.

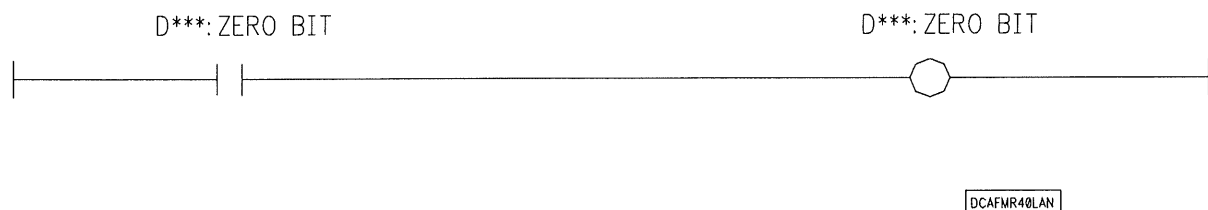


Figure 3-1. ADDvantage-32 Logic Diagram (sheet 14 of 14)

### 3.7 RUN, THREAD, AND JOG INPUTS

#### Y\*\*\* Parameters

Y\*\*\*:RUN INPUT

Y\*\*\*:JOG INPUT

Y\*\*\*:THRD INPUT

These three parameters enable the control loops of the ADDvantage-32. Each parameter can be configured to a value in the digital data table which enables its particular function. These three parameters are interlocked. Therefore, only one can be enabled at a time. Consult the Logic Sequence description provided in this section for specific interlock information.



Example: Assume the following inputs are being used to run, jog, or thread the section:

Digital Input 1 = Run Section  
 Digital Input 2 = Jog Section  
 Digital Input 3 = Thread Section

1. The values for the three digital inputs in the Digital Data Table are: D\*\*\*:USER 1 for digital input 1, D\*\*\*:USER 2 for digital input 2, and D\*\*\*:USER 3 for digital input 3.
2. Configure the parameters as follows:

Y\*\*\*:RUN INPUT = D\*\*\*:USER 1  
 Y\*\*\*:JOG INPUT = D\*\*\*:USER 2  
 Y\*\*\*:THRD INPUT = D\*\*\*:USER 3

### 3.8

#### ANALOG INPUTS

##### X\*\*\* Parameters

X\*\*\*:INPT #1 CAL  
 X\*\*\*:INPT 1 ZERO  
 X\*\*\*:INPT #1 TC  
 X\*\*\*:INPT #2 CAL  
 X\*\*\*:INPT #2 ZERO  
 X\*\*\*:INPT #2 TC  
 X\*\*\*:INPT #3 CAL  
 X\*\*\*:INPT #3 ZERO  
 X\*\*\*:INPUT #3 TC  
 X\*\*\*:INPUT #4 CAL  
 X\*\*\*:INPUT #4 ZERO  
 X\*\*\*:INPUT #4 TC  
 X\*\*\*:INPUT #5 CAL  
 X\*\*\*:INPUT #5 ZERO  
 X\*\*\*:INPUT #5 TC  
 X\*\*\*:INPT #6 CAL  
 X\*\*\*:INPT #6 ZERO  
 X\*\*\*:INPT #6 TC

##### A\*\*\* Parameters

A\*\*\*:ANALOG IN 1  
 A\*\*\*:ANALOG IN 2  
 A\*\*\*:ANALOG IN 3  
 A\*\*\*:ANALOG IN 4  
 A\*\*\*:ANALOG IN 5  
 A\*\*\*:ANALOG IN 6

There are six -10 to +10 VDC analog inputs located on the ADDvantage-32 maxi system board. Each input is scanned, calibrated, and written into the analog data table to be used by the application software every SCR firing. The value of the input is determined by the following equation:

$$A^{***}:ANALOG\ IN\ 1 = \\ Input\ Volts\ (X^{***}:INPT\ \#1\ CAL) + X^{***}:INPT\ 1\ ZERO$$

For example, to scale analog input #1 so that a -10 VDC to 10 VDC signal reads 0 to 2500 FPM in the analog data table, perform the following:

1. Find A<sup>\*\*\*</sup>:ANALOG IN 1 in the analog data table.
2. Use this information in the following equations:

$$\begin{aligned} 0\ FPM &= -10VDC\ (X^{***}:INP\ \#1\ CAL) + X^{***}:INPT\ 1\ ZERO \\ 2500\ FPM &= 10VDC\ (X^{***}:INP\ \#1\ CAL) + X^{***}:INPT\ 1\ ZERO \end{aligned}$$

Solving the above equations yields the following results:

$$\begin{aligned} X^{***}:INPT\ \#1\ CAL &= 125\ FPM/VDC \\ X^{***}:INPT\ 1\ ZERO &= 1250\ FPM \end{aligned}$$

### NOTE

The zero value is limited to 150 times the CAL value. Erroneous results will occur if this is exceeded.

## 3.9 ANALOG OUTPUT FUNCTIONS

### X<sup>\*\*\*</sup> Parameters

X<sup>\*\*\*</sup>:OUTPT 1 CAL  
X<sup>\*\*\*</sup>:OUTPT 1 ZER  
X<sup>\*\*\*</sup>:OUTPT 2 CAL  
X<sup>\*\*\*</sup>:OUTPT 2 ZER  
X<sup>\*\*\*</sup>:OUTPT 3 CAL  
X<sup>\*\*\*</sup>:OUTPT 3 ZER  
X<sup>\*\*\*</sup>:OUTPT 4 CAL  
X<sup>\*\*\*</sup>:OUTPT 4 ZER

### Y<sup>\*\*\*</sup> Parameters

Y<sup>\*\*\*</sup>:ANLG OUT 1  
Y<sup>\*\*\*</sup>:ANLG OUT 2  
Y<sup>\*\*\*</sup>:ANLG OUT 3  
Y<sup>\*\*\*</sup>:ANLG OUT 4

Analog outputs read information from the analog data table, scale it, and produce a -10 VDC to +10 VDC output signal. Each analog output is configurable to any data table value. The output is then scaled by the following function:

$$Output\ VDC = (Data\ Table\ Value + X^{***}:OUTPUT\ 1\ ZERO) X^{***}:OUTPT\ 1\ CAL$$

For example, to generate a -10 VDC to +10 VDC signal from the the second analog output of the ADDvantage-32 system board which represents actual speed (0 - 2500 FPM), perform the following:

1. Find A\*\*\*:ACT SPEED in the analog data table.
2. Configure Y\*\*\*:ANLG OUT 2 to A\*\*\*:ACT SPEED. This will send the output to the second analog output.
3. Find the calibration values as follows:

$$\begin{aligned} -10\text{VDC} &= (0 \text{ FPM} + \text{X***:OUTPUT 1 ZERO})(\text{X***:OUTPT 1 CAL}) \\ +10\text{VDC} &= (2500 \text{ FPM} + \text{X***:OUTPUT 1 ZERO})(\text{X***:OUTPT 1 CAL}) \end{aligned}$$

Solving the above equations yields the following:

$$\begin{aligned} \text{X***:OUTPT 1 CAL} &= .008 \text{ VDC/FPM} \\ \text{X***:OUTPT 1 ZERO} &= -1250 \text{ FPM} \end{aligned}$$

### 3.10 FREQUENCY INPUTS

<u>X*** Parameters</u>	<u>Y*** Parameters</u>	<u>A*** Parameters</u>
X***:TACH 1 GRat	Y***:TACH 1 TYPE	A***:SPEED IN 1
X***:TACH 1 RDia	Y***:TACH 2 TYPE	A***:SPEED IN 2
X***:TACH 1 EPR		
X***:TACH 1 ZERO		
X***:TACH 2 GRat		
X***:TACH 2 RDia		
X***:TACH 2 EPR		
X***:TACH 2 ZERO		

Frequency inputs convert an incoming pulse train into an analog value by counting the number of pulse edges and calibrating it into a user value. Counting the number of edges allows for a more accurate representation of the incoming pulse train. The analog value is then stored in the analog data table.

There are two methods used for counting the pulse train edges: the averaging method and the direct count method. Configuring Y\*\*\*:TACH 1 TYPE or Y\*\*\*:TACH 2 TYPE determines which method is used. Both methods measure one or two phase inputs and one or two pulse edges.

### 3.10.1 AVERAGING METHOD (TWO PHASE, 1 PHASE 2X, 1 PHASE 1X)

When one of these options is selected for the TACH TYPE, the pulse train edges are counted and averaged over an internal sample period. This averaging method allows for smoother control but can lead to inaccuracies if the duty cycle of the pulse is not 50/50. Selection of the 1 PHASE 1X (one edge) option eliminates these inaccuracies but decreases the resolution. This method should be used when the frequency input is used for speed feedback and the frequency being applied is fairly low. It should also be used for feedback applications that have significant cyclical resonance on the feedback.

### 3.10.2 DIRECT COUNT METHOD (TWO PHASE-S, 1 PHASE-2XS, 1 PHASE-1XS)

If one of these options for TACH TYPE is selected, the exact number of edges that occur in the same internal sample period are counted. This method leads to a more accurate count of the pulse train input but is not quite as smooth as the above method. This method should be used for all applications other than those stated for the averaging method.

Calibrate the pulse train into a user value by using the following equation:

A\*\*\*:SPEED IN 1=

$$\frac{[(\text{INPUT FREQ}) \times (\text{EDGE/PULSE}) + (\text{TACH 1 ZERO})] \times (60) \times (\pi) \times (\text{TACH 1 RDia})}{(\text{TACH 1 EPR}) \times \text{TACH 1 GRat}}$$

EDGES/PULSE = 1 is used for one phase, one edge applications  
 2 is used for one phase, two edge applications  
 4 is used for two phase, two edge applications

For example, to calibrate the frequency input into feet per minute from the following machine data:

2-phase, 240 PPR pulse generator mounted on the motor shaft  
 3.0 gear ratio from motor to roll  
 Roll diameter of 24 inches

1. Select the tach type required by setting Y\*\*\*:TACH 1 TYPE=Q\*\*\*:2 PHASE-S or Q\*\*\*:TWO PHASE.
2. Set X\*\*\*:TACH EPR = 960. Pulses per revolution of the pulse generator times four edges per pulse.
3. Set X\*\*\*:TACH GRat = 3.0 per the given machine data.
4. Set X\*\*\*:TACH RDia = 2, which is the diameter of the roll in process units (feet).

### 3.11 COUNTERS

<u>X*** Parameters</u>	<u>Y*** Parameters</u>	<u>Analog Data Table</u>
X***:COUNT 1 CAL	Y***:CTR 1 RESET	A***:FOOTAGE 1
X***:COUNT 2 CAL	Y***:CTR 1 HOLD	A***:FOOTAGE 2
	Y***:CTR 2 RESET	A***:DIF FOOTAGE
	Y***:CTR 2 HOLD	
	Y***:DIF-CTR RST	
	Y***:DIF-CTR HLD	

The frequency inputs correspond to an associated counter. The counter increases one unit for every pulse edge detected. The increment value is determined as follows:

$$A***:FOOTAGE 1 = (1, 2 \text{ or } 4 \text{ Edges/Pulse}) (\text{Pulses}) X***:COUNT 1 CAL$$

Where: 1 - Is used when the frequency input is set up for 1 PHASE, one edge operation.

2 - Is used when the frequency input is set up for 1 PHASE, two edge operation.

4 - Is used when the frequency input is set up for 2 PHASE, two edge operation.

Each counter can be reset or held by configuring Y\*\*\*:CTR 1 RESET and Y\*\*\*:CTR 1 HOLD to the appropriate bit in the digital data table.

For example, a 2-phase tach is connected to frequency input number 2 and produces 750 pulses for every foot of product. A reset button is wired into the first digital input on the system board. The counter is to be held any time the second digital input is on. To calibrate and configure the counter to count inches of product, perform the following:

1. Locate D\*\*\*:USER 1 and D\*\*\*:USER 2, the parameters in the digital data table which represent the two digital inputs being used.
2. Configure Y\*\*\*:CTR 2 RESET to D\*\*\*:USER 1. Configure Y\*\*\*:CTR 2 HOLD to D\*\*\*:USER 2.

This will reset the counter when the first digital input turns on and will hold the counter when the second input is on.

3. To determine the calibration number for the counter, the length per pulse must be found. It is given that 750 pulses = 1 foot. Converting this into inches yields:

$$\frac{750 \text{ pulses/ft}}{12 \text{ inch/ft}} = 62.5 \text{ pulses/inch}$$

or

$$1 \text{ pulse} = 1/(62.5 \text{ pulses/inch}) = .016 \text{ inches}$$

The increment value for the counter is .016 inches every pulse. To determine the calibration parameter, set the equation up for one increment value as follows:

$$A^{***}:FOOTAGE\ 2 = .016 \text{ inches/pulse} = (4) * X^{***}:COUNT\ 2\ CAL/PULSE$$

$$X^{***}:COUNT\ 2\ CAL = .004$$

This value causes the counter to increment 0.016 inches for every pulse detected at the frequency input.

The differential footage counter keeps track of the difference between the two frequency inputs.

$$A^{***}:DIF\ FOOTAGE =$$

$$(1, 2, \text{ or } 4 \text{ EDGES/PULSE})(PULSES\ FREQ\ IN1)(X^{***}:COUNT\ 1\ CAL)$$

$$- (1, 2, \text{ or } 4 \text{ EDGES/PULSE})(PULSES\ FREQ\ IN2)(X^{***}:COUNT\ 2\ CAL)$$

The above equation is modified every one million counts to prevent counter overflows. This will cause a small floating point error at this event.

When Y<sup>\*\*\*</sup>:DIF - CTR RST is high, the differential footage counter is reset.

When Y<sup>\*\*\*</sup>:DIF - CTR HLD is high, the differential footage counter is held.

### 3.12

## HARDWARE CONFIGURATION AND DIAGNOSTIC PARAMETERS

<u>X<sup>***</sup> Parameters</u>	<u>Y<sup>***</sup> Parameters</u>	<u>A<sup>***</sup> Parameters</u>	<u>D<sup>***</sup> Parameters</u>
X <sup>***</sup> :I/O V-REF	Y <sup>***</sup> :DRIVE P/N	A <sup>***</sup> :LINE VOLTS	D <sup>***</sup> :REV LOCKOUT
X <sup>***</sup> :ANLG FSCALE	Y <sup>***</sup> :BRG SELFTST	A <sup>***</sup> :LINE FREQ	D <sup>***</sup> :LINE IMBAL
	Y <sup>***</sup> :4Q OPERATE		D <sup>***</sup> :ABC ROTATE
	Y <sup>***</sup> :LINK BAUD		D <sup>***</sup> :PHA LOSS PT
	Y <sup>***</sup> :ANLG DISPLY		D <sup>***</sup> :PHB LOSS PT
			D <sup>***</sup> :PHC LOSS PT
			D <sup>***</sup> :LOW FREQ PT
			D <sup>***</sup> :HI FREQ PT
			D <sup>***</sup> :SCR ENABLE

Hardware configuration parameters are used to set up fundamental operations of the ADDvantage-32. Refer to Appendix C for an explanation of these parameter functions.

### 3.13 USER FAULT INPUTS

#### Y\*\*\* Parameters

Y\*\*\*:USR FAULT 1  
 Y\*\*\*:USR FAULT 2  
 Y\*\*\*:USR FAULT 3  
 Y\*\*\*:USR FAULT 4  
 Y\*\*\*:USR FAULT 5  
 Y\*\*\*:USR FAULT 6  
 Y\*\*\*:USR FAULT 7  
 Y\*\*\*:USR FAULT 8

User fault inputs allow the user to enable fault conditions beyond those generated internally by the ADDvantage-32. When the fault condition occurs, the ADDvantage-32 faults out and a message is stored in the FAULT FIFO. The ADDvantage-32 must be reset before operating again.

For example, two of the most common user faults are overspeed and tach loss conditions. To set up the ADDvantage-32 to fault on these two conditions, perform the following:

1. Find D\*\*\*:OVER SPEED and D\*\*\*:TACH LOSS, the two parameters in the digital data table that represent overspeed and tach loss.
2. Configure D\*\*\*:OVER SPEED to Y\*\*\*:USR FAULT 1. Configure D\*\*\*:TACH LOSS to Y\*\*\*:USR FAULT 2.

When either one of these conditions occurs, the ADDvantage-32 faults out.

### 3.14 MOTOR PARAMETERS

#### X\*\*\* Parameters

X\*\*\*:MOTOR IARM  
 X\*\*\*:MOTOR IFLD  
 X\*\*\*:MFLD % SCALE  
 X\*\*\*:MFLD ASCALE  
 X\*\*\*:FLD RESIST

#### Y\*\*\* Parameters

Y\*\*\*:FIELD CNTRL

#### A\*\*\* Parameters

A\*\*\*:FIL ARM CUR  
 A\*\*\*:ARM CURRNT  
 A\*\*\*:ARM CURRENT  
 A\*\*\*:FLD CURRENT  
 A\*\*\*:FLD CURRNT  
 A\*\*\*:MOTOR CEMF

Motor parameters are used to determine the amount of armature and field current being supplied to the motor. The ADDvantage-32 current is scaled to the motor current using the following equations:

$$X^{***}: \text{MOTOR IARM} = \frac{\text{Rated Motor Armature Current}}{\text{Rated ADDvantage-32 Current}} \times 100$$

$$X^{***}: \text{MOTOR IFLD} = \frac{\text{Rated Motor Field Current}}{\text{Rated ADDvantage-32 Current}} \times 100$$

Y^{\*\*\*}:FIELD CNTRL - Enables the field bridge. If an external field supply is used, disable this function.

\*\*\*\*\*

### WARNING

DISABLING THE FIELD CONTROL CAUSES THE MOTOR TO RUN AWAY IF AN EXTERNAL SOURCE IS NOT PRESENT. INTERLOCKS SHOULD BE SET UP SO THAT IF THE EXTERNAL SOURCE NO LONGER FUNCTIONS, THE ADDvantage-32 FAULTS OUT.

\*\*\*\*\*

For example, an ADDvantage-32 rated for 56 ADC will be used to operate a motor with a 40 ADC armature and a 2 ADC field. Set up the parameters for this motor as follows.

1. Enable Y^{\*\*\*}:FIELD CNTRL.
2. Calculate X^{\*\*\*}:MOTOR IARM as follows:

$$X^{***}: \text{MOTOR IARM} = \frac{40 \text{ ADC}}{56 \text{ ADC}} \times 100\%$$

$$X^{***}: \text{MOTOR IARM} = 71.43\%$$

3. An ADDvantage-32 rated at 56 ADC can provide a maximum of 6 ADC to a motor field. Calculate X^{\*\*\*}:MOTOR IFLD as follows:

$$X^{***}: \text{MOTOR IFLD} = \frac{2 \text{ ADC}}{6 \text{ ADC}} \times 100\%$$

$$X^{***}: \text{MOTOR IFLD} = 33.33\%$$



X\*\*\*:MFLD %SCALE is a scaling factor for percentage field amps vs. feedback CT voltage. The UL field supply for the 180 amp drive needs this changed to 1.0416. (Chassis P/N D22976, included in all new drives). For AFM applications, the drive expects 2 volts feedback equal to 100% field bridge current. Adjust this parameter to correct the percentage; e.g., if 1 volt = 100%, enter  $(2 \text{ volts}/1 \text{ volt}) = 2$ .

X\*\*\*:MFLD ASCALE is a scaling factor for full field amps vs. feedback CT voltage. The UL field supplies for the 56 amp and 180 amp drive needs this changed to 2 and 2.083 respectively (Chassis P/N D22974 and D22976, included in all new drives). For 540, 850, and 1350 amp drives, a 12 amp field supply is expected. For 1550-3000 amp drives, a 24 amp field supply is expected.

If a drive is equipped with a different amp field supply, this parameter needs to be adjusted; e.g., if an 850 amp drive is equipped with a 24 amp field supply, enter  $(24 \text{ amps}/12 \text{ amps}) = 2$ . (See Section 1.4 Identification of Part Numbers for full field rating.)

For AFM applications, the drive expects 2 volts feedback equal to a 12 amp field supply. Adjust to correct for proper amperage; e.g., if 2 volts = 48 amps, enter  $(48 \text{ amps}/12 \text{ amps}) = 4$ .

If the field current required is greater than the ADDvantage-32 rating, modifications can be made. Consult the factory for additional information.

### 3.15

#### MOTOR THERMAL SETTINGS

##### X\*\*\* Parameters

X\*\*\*:THERMAL TC  
X\*\*\*:M-TEMP WARN  
X\*\*\*:RBRDF RATIO

##### A\*\*\* Parameters

A\*\*\*:MOTOR TEMP  
A\*\*\*:HEATSK TEMP  
A\*\*\*:IIR INTEGR

##### D\*\*\* Parameters

D\*\*\*:M-TEMP WARN  
D\*\*\*:HS TMP WARN

Thermal capacity of the ADDvantage-32 and motor is represented by two internal counters called I<sup>2</sup>R (IIR, as shown in drive) integrators. Any time the ADDvantage-32 drive or the motor is operating over 110% of full load, its counter starts to count up. If an integrator reaches 100, then the drive will fault and shut down. If the current goes below its 110% rating, its counter will start to count down until it reaches zero.

There is a scaling factor for the drives thermal protection on the reverse bridge. On AFM applications, the reverse bridge may only be used for jog reverse and be sized smaller than the forward bridge. Set X\*\*\*:RBRDG RATIO to the forward bridge capacity over the reverse bridge capacity.

The hardware is also protected by a thermocouple that monitors the SCR heat sink temperature. If the heat sink gets too hot, the ADDvantage-32 faults out.

Motor temperature can also be monitored by the ADDvantage-32. This is done by determining the present motor field resistance and comparing it to the original value. An increase in resistance signifies an increase in motor temperature. The ADDvantage-32 takes the difference between the two values and calculates the temperature (A\*\*\*:MOTOR TEMP).

X\*\*\*:THERMAL TC - Used to set up the IIR integrator for the motor (A\*\*\*:IIR INTEGR), it is the amount of time the ADDvantage-32 can operate at 150% rating before a value of 100 is obtained. A value of 60 seconds at 150% will allow the motor 8 seconds at 200%. A value of 425 seconds at 150% will allow the motor 60 seconds at 200%. (See the following chart.)

X\*\*\*:M-TEMP WARN - This parameter is used to generate the warning bit D\*\*\*:M-TEMP WARN. When the calculated motor temperature goes above this value, D\*\*\*:M-TEMP WARN turns on. This bit could then be configured to a user fault or a digital output to display a warning. This temperature is calculated from the change in field resistance.

The drive IIR is not settable and is set to fault when the drive is R/A outputting 150% of the rated bridge for 60 seconds. On non-UL AFM applications, this can be disabled by the factory.

There are three possible IIT curves to choose from: one that trips after 8 seconds of 200%, one that trips after 10 seconds of 250%, and one that trips after 10 seconds of 300%. See Figure 3-2B.

Use parameter Y\*\*\*: IIT CURVE to select the desired curve.

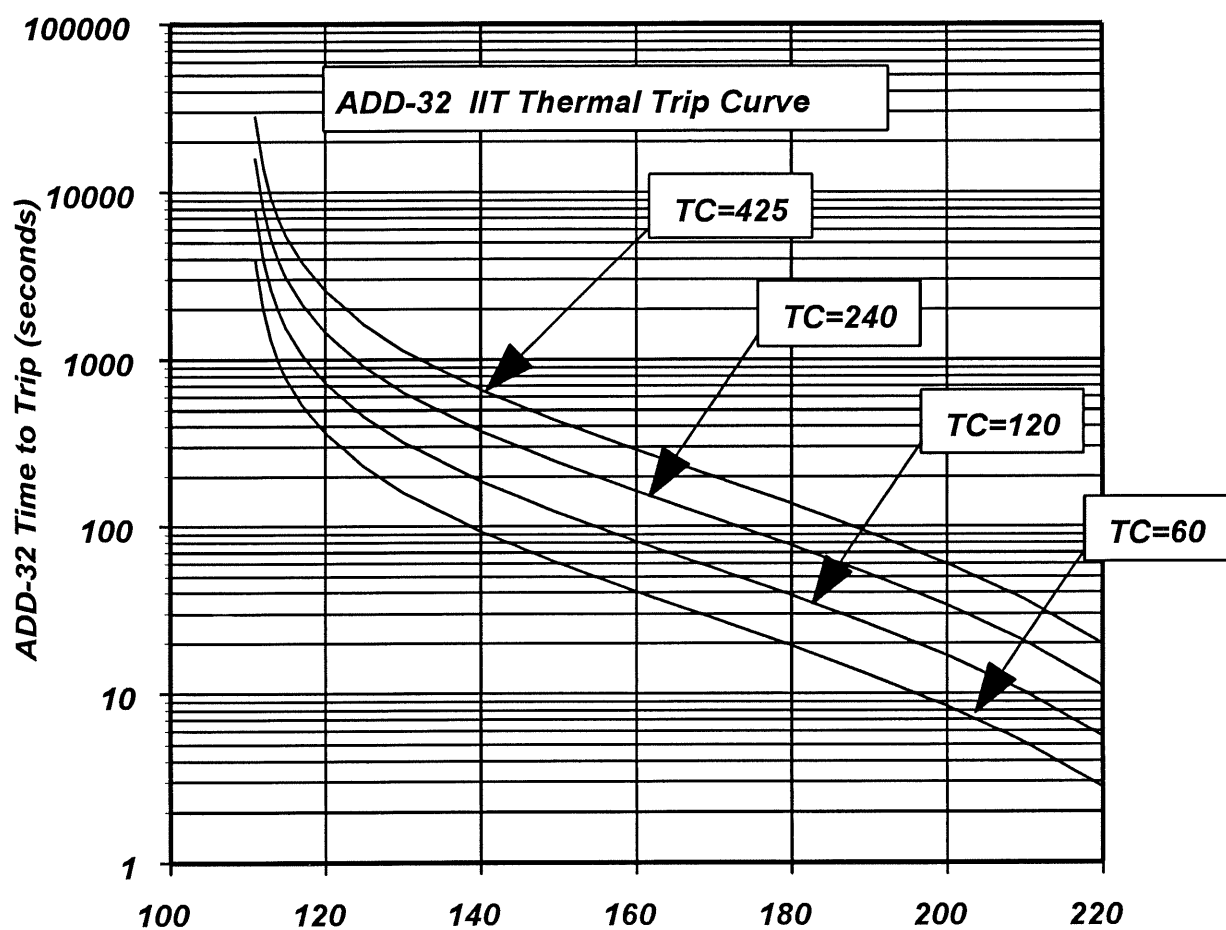


Figure 3-2A. Motor Temperature Overload Curve

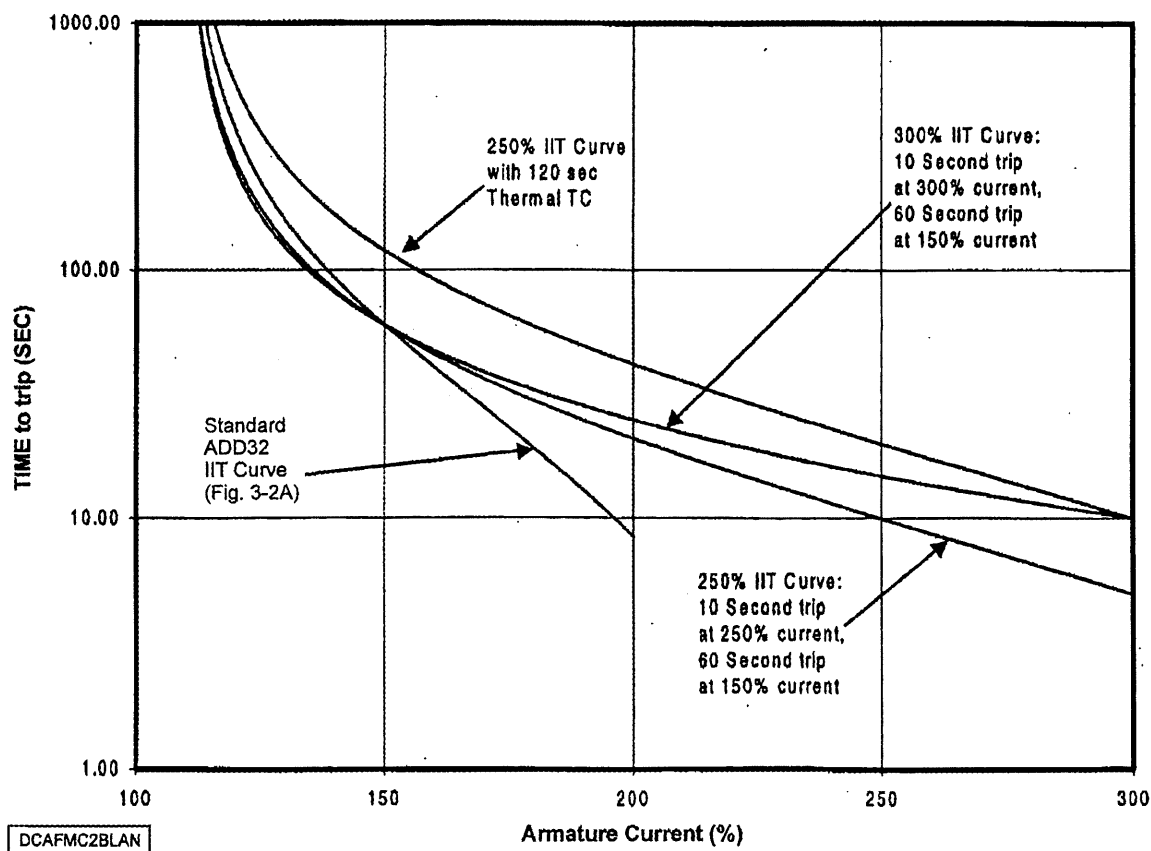


Figure 3-2B. Selectable IIT Curves

## 3.16

## CURRENT LOOP PARAMETERS

X\*\*\* Parameters

X\*\*\*:IARM CONTIN  
 X\*\*\*:MAX ARM ALP  
 X\*\*\*:MIN ARM ALP  
 X\*\*\*:ARM RESIST  
 X\*\*\*:Z-C CORRECT  
 X\*\*\*:IARM PGAIN  
 X\*\*\*:IARM IGAIN  
 X\*\*\*:IARM D-BAND  
 X\*\*\*:IARM R-LIM

Y\*\*\* Parameters

Y\*\*\*:IARM PI CTL  
 Y\*\*\*:IARM FFWD  
 Y\*\*\*:Ia RATE SEL

A\*\*\* Parameters

A\*\*\*:VARM CMD  
 A\*\*\*:ARM ALPHA  
 A\*\*\*:PCNT DISCON  
 A\*\*\*:IARM CMD  
 A\*\*\*:IARM SETPT  
 A\*\*\*:IARM ERROR  
 A\*\*\*:IARM INTEG  
 A\*\*\*:POS I LIMIT  
 A\*\*\*:NEG I LIMIT

D\*\*\* Parameters

D\*\*\*:MAX A ALPHA  
 D\*\*\*:MIN A ALPHA  
 D\*\*\*:IARM MIN PT  
 D\*\*\*:IARM I HOLD  
 D\*\*\*:IARM I RES  
 D\*\*\*:MAX IARM  
 D\*\*\*:MIN IARM

The current loop is the most fundamental control loop in the ADDvantage-32. It provides digital control for the SCR circuitry. Figure 3-3 is a block diagram of the current loop.

Using the Self Tune function automatically tunes the current loop for the connected motor. The five parameters tuned are as follows:

- |                                      |   |
|--------------------------------------|---|
| X***:IARM CONTIN -                   | This parameter represents the percent motor current at which continuous conduction of the current occurs.   |
| X***:Z-C CORRECT -                   | To fire the SCR's properly, the point at which the line voltage crosses zero must be determined. Due to delays in the sensing circuitry, an offset number must be entered. X***:Z-C CORRECT is the value used to offset this delay. |
| X***:IARM PGAIN -<br>X***:IARM IGAIN | These are the proportional and integral gain constants for the current loop. They determine how the current loop reacts to disturbances.  |
| X***:ARM RESIST -                    | This is the value of the armature resistance in ohms.   |

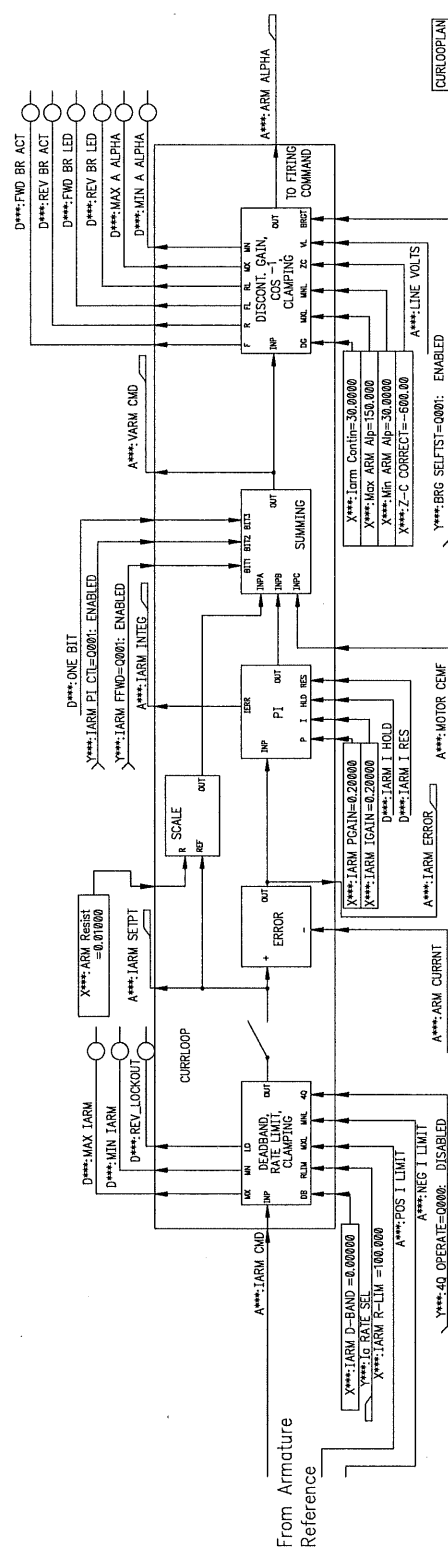


Figure 3-3. Current Loop Block Diagram

Several other parameters are provided for current loop operation. For most applications, these parameters do not change.

Y***:IARM PI CTL -	Enables or disables the proportional and integral gain in the current loop. (Normally enabled.)
Y***:IARM FFWD -	Enables or disables the feed forward gain in the current loop. Feed forward gain enhances the response of the loop (normally enabled) and enables the drive to start into a spinning motor.
Y***:Ia RATE SEL -	Selects the value used for armature current rate of change limit. Usually left = to X***:IARM R-LIM unless a non-linear value is required.
X***:MAX ARM ALP -	Sets the maximum allowable angle at which the armature SCR's fire. This parameter should never be changed without first consulting the factory.
X***:MIN ARM ALP -	Sets the minimum allowable angle at which the armature SCR's fire. This parameter should never be changed without first consulting the factory.
X***:IARM D-BAND -	Dead band range entered in percent motor current is used in situations where a motor is jittery at zero speed.
X***:IARM R-LIM -	This is the allowable rate at which the current reference changes per sample time (2.77 ms on 60 Hz systems). This value is entered in percent motor current and is normally 100%.

### 3.17

#### FIELD CURRENT LOOP PARAMETERS

<u>X*** Parameters</u>	<u>Y*** Parameters</u>	<u>A*** Parameters</u>	<u>D*** Parameters</u>
X***:MAX FLD ALP	Y***:FLD B-TYPE	A***:FLD CURRENT	D***:FLD LOSS PT
X***:MIN FLD ALP	Y***:FLD V-CMD	A***:FLD CURRNT	D***:FLD ECON PT
X***:FLD TX RAT		A***:FLD VOLTS	D***:FLD TIMER
X***:FLD LOSS		A***:VFLD CMD	D***:FLD OK PT
X***:FLD PHASE		A***:FLD ALPHA	D***:FLD ENABLE
X***:IFLD PGAIN		A***:IFLD CMD	D***:FLD CTL LOS
X***:IFLD IGAIN			

The ADDvantage-32 comes supplied with a single phase motor field supply. See drive rating for full rating of the supply. The standard hardware configuration is a two SCR, two diode bridge. An optional four SCR bridge can be supplied.

The following parameters set up the field current loop control.

Y***:FLD B-TYPE -	Select to the hardware supplied, either two or four SCR field bridge. Standard is two SCR bridge.
Y***:FLD V-CMD -	Defaulted to be the output of the field current loop. If field voltage control is desired, reconfigure this to a field voltage reference. Note field loss protection is disabled as soon as this is changed from default.
X***:MAX FLD ALP -	Set to the maximum allowable angle at which the field SCR's can fire. This parameter should never be changed without first consulting the factory.
X***:MIN FLD ALP -	Set to the minimum allowable angle at which the field SCR's can fire. This parameter should never be changed without first consulting the factory.
X***:FLD TX RAT -	Set to the ratio of the field supply input voltage vs. the armature supply input voltage. Used if a step down transformer is needed to feed the field supply.
X***:FLD LOSS -	Set to the percentage of full field current used to trip the drive out on field loss fault. Defaulted to 25% of full rating.
X***:FLD PHASE -	Degree out of phase the field voltage is from the armature. Consult Avtron Industrial Automation, Inc., if the field is supplied from a separate source.
X***:IFLD PGAIN -	Proportional gain constant for the field current loop. Default is adequate for most motors.
X***:IFLD IGAIN -	Integral gain constant for the field current loop. Default is adequate for most motors. Gain is entered in seconds per repeat.



### 3.18 MOTOR STALL PROTECTION

#### X\*\*\* Parameters

X\*\*\*:STALL SPEED  
X\*\*\*:STALL % AMP  
X\*\*\*:STALL TIME

#### Y\*\*\* Parameters

Y\*\*\*:STALL PROT

#### D\*\*\* Parameters

D\*\*\*:MOTOR STALL

Motor stall is used to protect a motor that is frozen or overloaded. If left in this condition, the motor can be permanently damaged.

Motor stall will fault out the drive if parameter Y\*\*\*:STALL PROT is enabled. A stall condition is realized when:

Actual % Armature Current	> X***:STALL % AMP
Motor Speed (In Process Units)	< X***:STALL SPEED
Elapsed Time	> X***:STALL TIME

When a motor stall is determined, digital data bit D\*\*\*:MOTOR STALL turns on regardless of Y\*\*\*:STALL PROT bit status. This bit can then be configured to a digital output for run removal.

### 3.19 AVTRON FIRING MODULE (DC0001-XXXX-X) OPTION

#### 3.19.1 General

#### X\*\*\* Parameters

X\*\*\*:BRIDGE SIZE  
X\*\*\*:ARM CT OUT  
X\*\*\*:AC VT SCALE  
X\*\*\*:DC VT SCALE

When using the ADDvantage-32 AFM (DC0001-XXXX-X) module, several parameters must be set so that the module can control the bridge current properly. The existing bridge's rating must be known as well as the turns ratio of the feedback CT's, the burden resistor value, and voltage feedback scaling. (Paragraph 3.19.3, AFM CURRENT TRANSFORMER PHASING PROCEDURE, has steps to determine or calculate necessary values, if unknown.) These values must be accurate or the bridge will not be controlled properly.

When a standard ADDvantage-32 is being used (DC0010 through DC2500), these parameters should be left at default.

The SCR Firing Adapter Module provides an interface to the existing power bridge. Refer to paragraph 3.19.3, AFM CURRENT TRANSFORMER PHASING PROCEDURE, for proper installation and setup. After completing the procedure, continue with Core Software Operation as you would for a standard ADDvantage-32 Power Converter.

\*\*\*\*\*

### WARNING

Setting these parameters incorrectly can result in loss of life as well as damage to equipment. Only qualified personnel should attempt any changes with these values.

\*\*\*\*\*

#### 3.19.2 Example Parameter Settings

For example, an AFM module is going to be installed with an existing 540 ADC rated bridge. The bridge has CT's with one turn on the primary and 4,000 turns on the secondary. A burden resistor across the CT is rated at 5 OHMS, 5 WATTS.

FOR THESE CONDITIONS, the parameters are set as follows:

#### BRIDGE RATING

X\*\*\*:BRIDGE SIZE=540 ADC

#### X\*\*\*:ARM CT OUT

$$\begin{aligned}
 X***: \text{ARM CT OUT} &= \frac{\text{CT Secondary Turns}}{\text{CT Primary Turns} * \text{Burden Resistor}} \\
 &= \frac{4000 \text{ Turns}}{1 \text{ Turn} * 5 \text{ Ohms}} \\
 &= 800
 \end{aligned}$$

X\*\*\*:AC VT SCALE

Ratio between sensed AC voltage and actual AC voltage. Leave at default except for high horsepower AFM applications. When 700 volts sense board P/N A22056 is used, set to 1.9926.

X\*\*\*:DC VT SCALE

Ratio between sensed DC voltage and actual DC voltage. Leave at default except for high horsepower AFM applications. When 700 volts sense board P/N A22056 is used, set to 1.9926.

3.19.3 AFM Current Transformer Phasing Procedure  
(A20651 SCR Firing Adapter Module)

\*\*\*\*\*

### WARNING

As an initial operation of any AFM startup, it is important to insure that the C.T.'s used to sense armature current are correctly phased.

\*\*\*\*\*

- 1) Before starting this procedure, the AFM wiring should be completely checked, drive power up complete, and proper drive software loaded.
- 2) Remove AFM power. Verify the correct part number and polarity of all current transformer assemblies. CT P/N = \_\_\_\_\_. Also document the burden resistor values, R = \_\_\_\_\_. If there is any question on the correct values for the burden resistors, go to the burden resistor calculation procedures starting at step 25.
- 3) Have a millwright lock the motor rotor. Uncouple motor only if there are felts or machinery sensitive to backward motion.
- 4) Connect test fixture/switchbox to the AFM. Terminate E-Stop wires marked 19 and 20 to TB1(19) and (20) or in series with other E-Stop pushbuttons already wired. Connect fixture Reset wires marked 17 and 18 to TB1(17) and (18).
- 5) Apply power to the AFM. Test E-Stop and E-Stop Reset functionality.

- 6) Enter the correct calibration values for the following parameters:

X\*\*\*:MFLD %SCALE = \_\_\_\_\_  
 X\*\*\*:BRIDGE SIZE = \_\_\_\_\_  
 X\*\*\*:ARM CT OUT = \_\_\_\_\_

- For AFM applications where the line voltage is above 600V, enter the correct scaling factors for the voltage sense circuits.

X\*\*\*:AC VT SCALE = \_\_\_\_\_  
 X\*\*\*:DC VT SCALE = \_\_\_\_\_

- 7) Configure the drive to have a current reference from a calibration parameter, and disable the CURRENT LOOP FFWD and SPEED LOOP.

- \* As an example, in the *Speed Loop* of 692002.V21 software, the TRQ REF SUM and D/DT SPD FFWD blocks can be configured to accomplish both tasks:

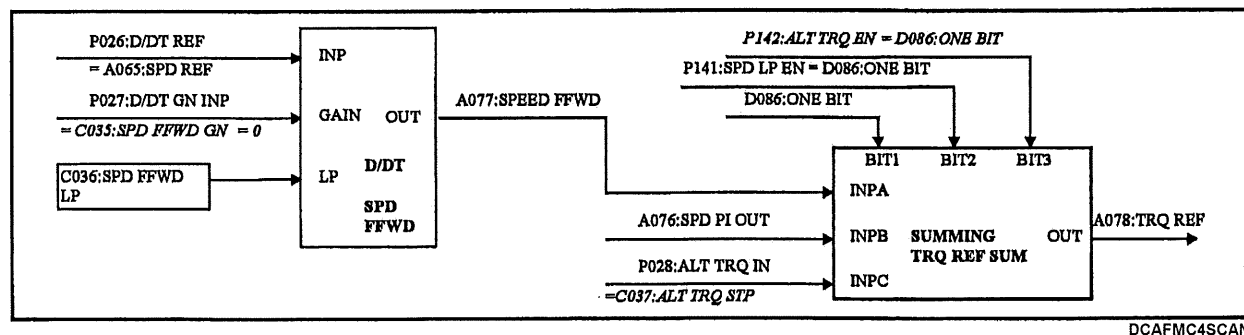


Figure 3-4. 692002.V21 Software Block Excerpt

- a) To configure the drive to have a current reference from a calibration parameter, (for this example), set  $P142:ALT TRQ EN = D086:ONE BIT$ . The desired armature current value can be obtained by entering the value into the calibration parameter  $C037:ALT TRQ STP$ .

Document Actual Calibration Parameter Used →

C \_\_\_\_: \_\_\_\_\_ = 0

- b) To disable the CURRENT LOOP FFWD (for this example), set the D/DT SPD FFWD gain to zero.  $C035:SPD FFWD GN = 0$
- c) To disable the SPEED LOOP (for this example), set the BIT2 of the TRQ REF summing block, parameter  $P141:SPD LP EN$ , to  $D087:ZERO BIT$ .

Document All Changes Made Completing Step 2:

PARAMETER	NEW VALUE	ORIGINAL VALUE
_____:	= _____	, _____
_____:	= _____	, _____
_____:	= _____	, _____

8) Set the following parameters:

PARAMETER	NEW VALUE	ORIGINAL VALUE
Y***:FIELD CNTL	= DISABLED	, _____
Y***:BRG SLFTST	= DISABLED	, _____
Y***:4Q OPERATE	= DISABLED	, _____
X***:ARM Resist	= 0.00	, _____
X***:Iarm Contin	= 100	, _____
X***:Z-C CORRECT	= -800	, _____
X***:IARM PGAIN	= 0.10	, _____
X***:IARM IGAIN	= 0.00	, _____

9) \*\*\*\* RESET DRIVE \*\*\*\*

- 10) Connect a scope to measure the voltage across one of the CT burden resistors. **Remember to use an isolation plug on scopes with ground prong on power cord.** If the burden resistors are located in an inaccessible area, the scope may be connected to the SCR Firing Adapter point to which the burden resistor/CT wiring terminates. (See AFM's electrical drawing set for correct interconnections.) Set the time sweep to 1ms per division, set the voltage scale to 0.5 volts per division, and set the scope sync to the line.
- 11) Observe the armature firing angle A016:ARM ALPHA under OPERATE → DRIVE ANALOG and insure that it is approximately 120 degrees. If the firing angle is significantly smaller, check that all analog values throughout the ARMATURE CURRENT LOOP are all zero.
- 12) Place a clamp-on ammeter on one of the armature leads. This meter will be used to insure that excessive current is not applied to the motor while phasing the CT feedback. Closely watch the ammeter current while performing the following step. The armature current should not rise above 10% of the motor nameplate armature current.

- 13) Turn the drive on while observing the scope. Apply a run command, such that the "RUNNING" LED is illuminated. Slowly increase the current command through the calibration parameter documented in step 7-a, while observing the scope. Stop increasing the current command when voltage pulses are observed on the scope. The observed waveform should resemble that of Figure 3-5.

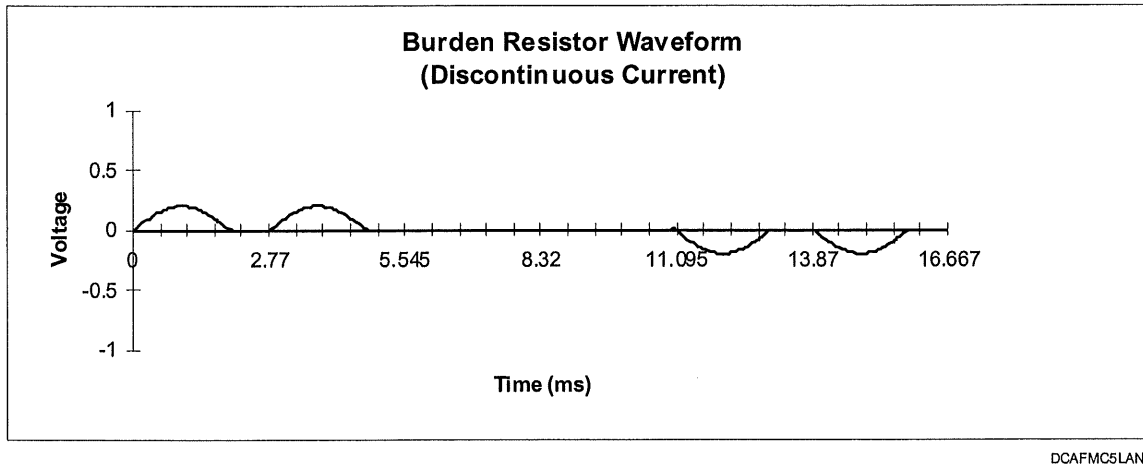


Figure 3-5. Burden Resistor Waveform (Discontinuous Current)

- 14) With an observable current flow at a burden resistor, move the scope probe to measure across the Iarm sense and common points on the bottom left of the microprocessor board. If all wiring and CT polarities are correct, the waveform should resemble that of Figure 3-6. If you observe this waveform, go to step 24, or continue on to step 15 if you **do not** observe this waveform.

NOTE THAT THERE IS A 5X GAIN BETWEEN THE CT BURDEN RESISTOR AND THIS POINT.

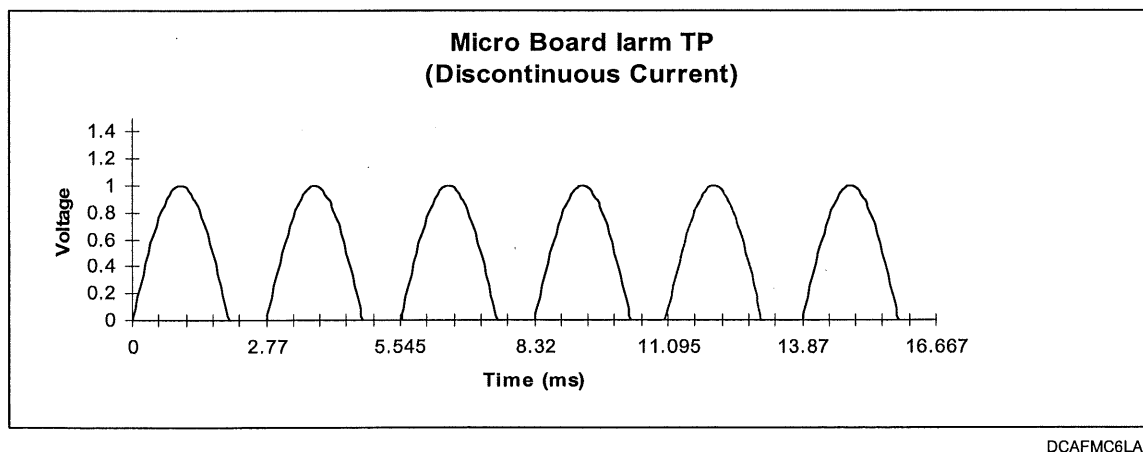


Figure 3-6. Micro Board Iarm TP (Discontinuous Current)

- 15) If no current is indicated on the microprocessor board, then check to insure that the PHASE A CT is connected to the PHASE A input on the FIRING MODULE, PHASE B CT is connected to the PHASE B input, and PHASE C CT is connected to the PHASE C input. Also check that the cables between the SCR Firing Adapter and the Field Supply Assembly are in place and secured by tightening screws on cable ends.
- 16) If the voltage observed on the scope is negative, instead of the positive pulses shown in Figure 3-6, reverse all CT polarities. If the CT leads are difficult to reach, switch the wires for all CTs at J1 of the SCR Firing Adapter.
- 17) If the voltage waveform observed on the scope has some positive segments and some negative segments as shown in Figure 3-7, then follow either the 3-CT or the 2-CT feedback phasing method, using the type your application has been configured with.

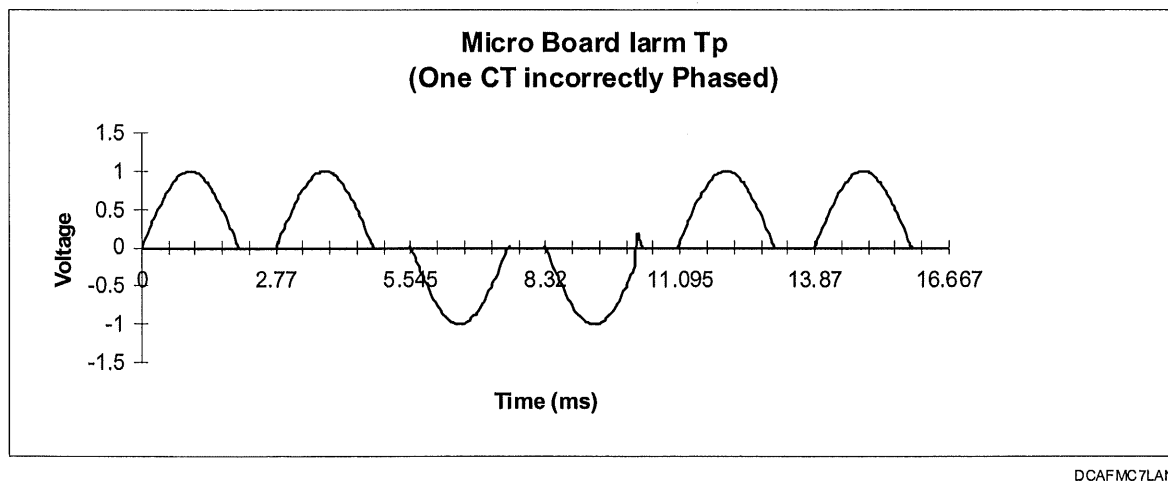


Figure 3-7. Micro Board Iarm TP  
(One CT Incorrectly Phased)

### 3-CT Feedback Phasing Method:

- 18) The 3-CT feedback configuration wiring diagram and jumper settings for the A20651 SCR Firing Adapter are shown in Figure 3-8. Check the polarity of the feedback pulses across each burden resistor with the polarities indicated for each resistor in Figure 3-8. Example: Positive pulses (Figure 3-4) should be observed for a burden resistor when the scope probe is connected to the resistor + and scope ground to the resistor -. Confirm these pulses at J1 of the SCR Firing Adapter. The burden resistor polarities are most easily identified here.

- 19) If any of the pulses are negative, switch the leads on the CT for that phase. If the CT leads are difficult to reach, switch the wires for this CT at J1 of the SCR Firing Adapter.
- 20) Return to step 14.

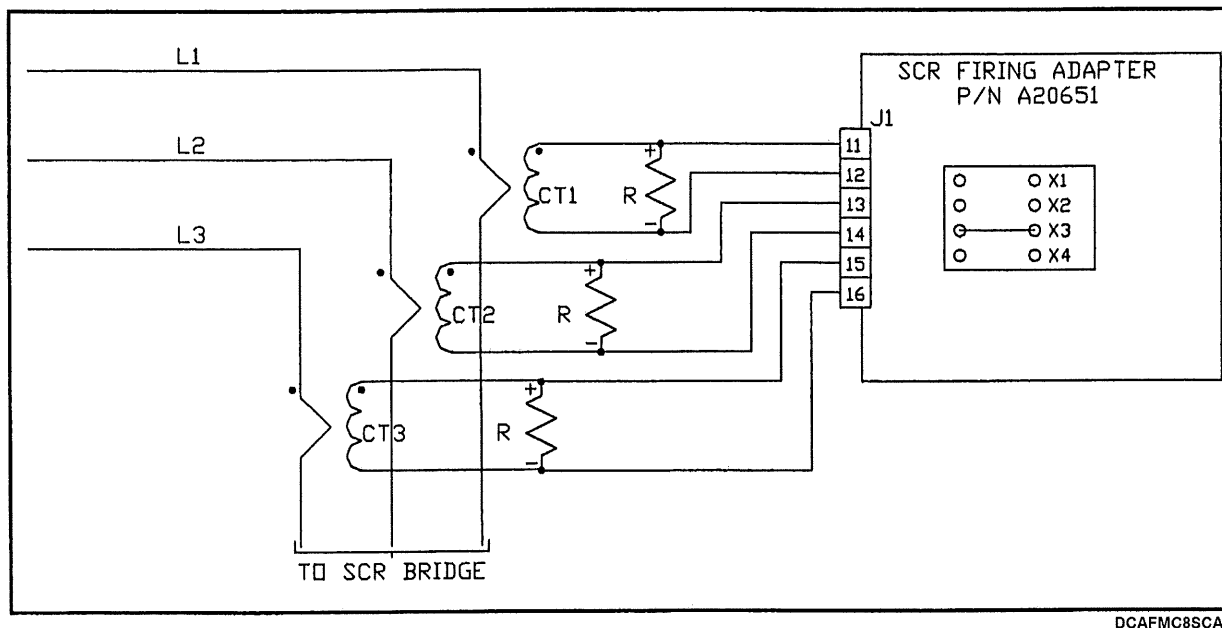
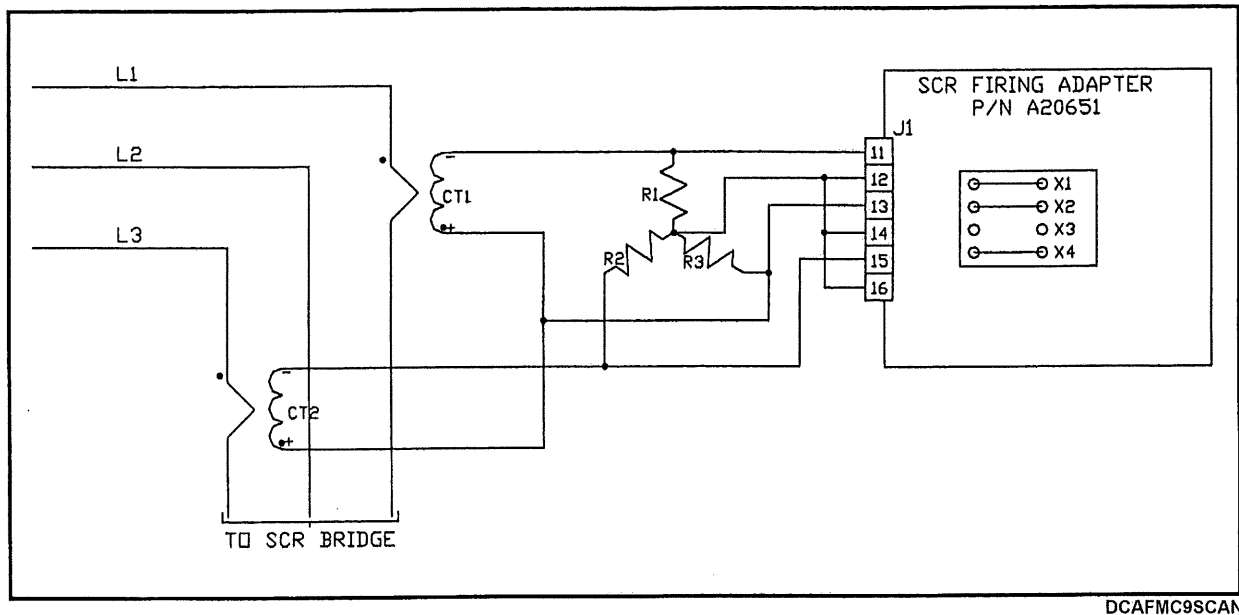


Figure 3-8. Firing Adapter 3-CT Configuration Diagram

### 2-CT Feedback Phasing Method:

- 21) The 2-CT feedback configuration wiring diagram and jumper settings for the A20651 SCR Firing Adapter are shown in Figure 3-9. Check the polarity of the feedback pulses across each burden resistor with the polarities indicated for each CT with the polarities indicated for each CT in Figure 3-8. Example: Positive pulses (Figure 3-4) should be observed for a CT when the scope probe is connected to the CT + and scope ground to the CT -. Confirm these pulses at J1 of the SCR Firing Adapter, points (13-11) for CT1 and J1(13-15) for CT2. The C polarities are most easily identified here.
- 22) Correct the CT polarities by switching the wire pair for the CT(s) whose feedback pulses are inverted from those shown in Figure 3-5.
- 23) Return to step 14.





DCAFM9SCAN

Figure 3-9. Firing Adapter 2-CT Configuration Diagram

- 24) Return the parameters changed in steps 7 and 8 back to their original values, reset drive and begin normal, non-AFM drive startup procedure. Continue on to step 25 if there is concern of having the incorrect burden resistor values.

### Calculating Burden Resistor Values:

- 25) For both the 2CT and 3CT configurations (see Figures 1-5 and 1-6), the following procedure applies to calculating burden resistor values. The value calculated below corresponds to all three resistors  $R1 = R2 = R3$ .
- 26) Obtain the current rating for the CT. This is usually given as a turns-ratio. This is equivalent to a ratio of input current to output current (Inpt Amps/Oupt Amps). Calculate and record the Output Amps of the CT for an input current equal to 300% full load motor current. As an example, for a CT with an 800A/1A rating, and rated motor armature current of 140A, the output of the CT at 300% motor current would be:

$$(1A/800A) * 140A * (300\%/100) = 0.525 \text{ Amps\_Out}$$

Actual CT output current at 300% motor current = \_\_\_\_\_ Amps.

- 27) The CT and burden resistor series circuit must produce 2V output given the current calculated in step 26. Calculate and document the resistance value that will produce 2V given the current of step 26. For the example above:

$$\left( \frac{2.0 \text{ Volts}}{0.525 \text{ Amps}} \right) = 3.81 \text{ Ohms}$$

Actual Burden Resistor value = \_\_\_\_\_ Ohms.

- 28) Perform a calculation for the power dissipation rating of the burden resistor ( $I^2R$ ). Use the current and resistance values calculated in steps 26 and 27. For the example calculation:

$$(0.525 \text{ Amps})^2 * (3.81 \text{ Ohms}) = 1.05 \text{ Watts}$$

As a precautionary measure, use a burden resistor with a power dissipation rating of at least twice the power dissipation rating calculated in step 28.

**AFM CT Ratio/Burden Resistor using Avtron stock CT's and "standard" burden values**

Goal is to scale burden for 0.667 V @ FLA or 2.0V at 300% FLA (IOC trip)

**600:1 CT p/n A18751**

Enter Drive FLA (DC) X061	CT Ratio (XXXX:1)	Pick & Enter Burden (Ohms)	CT Scale (A/Volt) X062	Actual IOC @ 2 VDC (ADC)	Calc. 300%FLA IOC (ADC)	Actual IOC (%)	Burden W @ 100 %	Burden W @ 300 %
100	600	4	150	300	300	300%	0.11	1.00
150	600	2.5	240	480	450	320%	0.16	1.41
200	600	2	300	600	600	300%	0.22	2.00
250	600	2	300	600	750	240%	0.35	3.12
300	600	1	600	1200	900	400%	0.25	2.25

**2500:1 CT p/n A18750**

Enter Drive FLA (DC) X061	CT Ratio (XXXX:1)	Pick & Enter Burden (Ohms)	CT Scale (A/Volt) X062	Actual IOC @ 2 VDC (ADC)	Calc. 300%FLA IOC (ADC)	Actual IOC (%)	Burden W @ 100 %	Burden W @ 300 %
200	2500	8	312	625	600	312%	0.05	0.46
300	2500	5	500	1000	900	333%	0.07	0.65
400	2500	4	625	1250	1200	312%	0.10	0.92
500	2500	3	833	1667	1500	333%	0.12	1.08
600	2500	2.5	1000	2000	1800	333%	0.14	1.30
700	2500	2.5	1000	2000	2100	286%	0.20	1.76
800	2500	2	1250	2500	2400	312%	0.20	1.84

**4000:1 CT p/n A19489**

Enter Drive FLA (DC) X061	CT Ratio (XXXX:1)	Pick & Enter Burden (Ohms)	CT Scale (A/Volt) X062	Actual IOC @ 2 VDC (ADC)	Calc. 300%FLA IOC (ADC)	Actual IOC (%)	Burden W @ 100 %	Burden W @ 300 %
300	4000	9	444	889	900	296%	0.05	0.46
350	4000	8	500	1000	1050	286%	0.06	0.55
400	4000	7	571	1143	1200	286%	0.07	0.63
500	4000	5	800	1600	1500	320%	0.08	0.70
600	4000	4	1000	2000	1800	333%	0.09	0.81
700	4000	4	1000	2000	2100	286%	0.12	1.10
800	4000	3	1333	2667	2400	333%	0.12	1.08
900	4000	3	1333	2667	2700	296%	0.15	1.37
1000	4000	2.5	1600	3200	3000	320%	0.16	1.41
1100	4000	2.5	1600	3200	3300	291%	0.19	1.70
1200	4000	2	2000	4000	3600	333%	0.18	1.62
1300	4000	2	2000	4000	3900	308%	0.21	1.90
1400	4000	2	2000	4000	4200	286%	0.24	2.20
1500	4000	2	2000	4000	4500	267%	0.28	2.53

**Notes:**

- 1) X062=CT ratio/R burden
- 2) Actual IOC=2 VDC \* X062
- 3) standard burdens are 9,8,7,6,5,4.5,4,3.5,3,2.5,2,& 1 Ohm--ref D27498-X Cur Fdbk Mod

### 3.20 RETENTIVE SETPOINTS

#### Y\*\*\* Parameters

Y\*\*\*: RET SETPT 1  
Y\*\*\*: RET SETPT 2  
Y\*\*\*: RET SETPT 3  
Y\*\*\*: RET SETPT 4  
Y\*\*\*: RET SETPT 5  
Y\*\*\*: RET SETPT 6

Retentive setpoints allow the user to store values from the analog patchboard (A\*\*\*) into memory to protect them against power loss. If a value is configured to the retentive parameter, it is copied into memory at power loss and then restored when power returns. The two footage counter values are also stored (A\*\*\*:FOOTAGE 1 and A\*\*\*:FOOTAGE 2).

For example, an exterior device is sending a setpoint to the ADDvantage-32 over the RS485 link or 802.4 LAN to A\*\*\*:LOCATION 1. If power is lost to the unit, the setpoint must be saved so that the section can operate at the same point it was when the power loss occurred. To achieve this, the following is required:

Configure Y\*\*\*:RET SETPT 1 = A\*\*\*:LOCATION 1

If a power loss occurs, the value will be stored and placed back into A\*\*\*:LOCATION 1 when power is restored.

## SECTION IV

### CONTROL BLOCK DESCRIPTION

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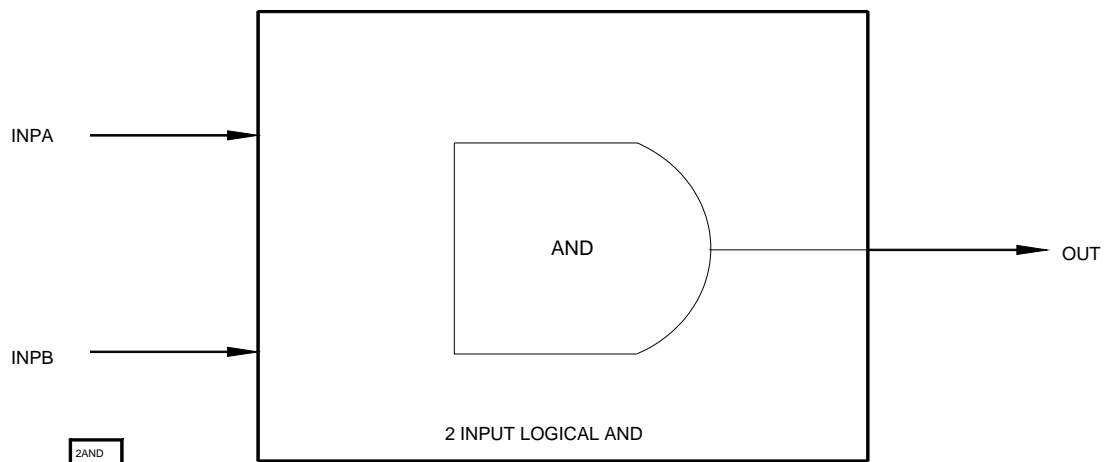
## SECTION IV

# CONTROL BLOCK DESCRIPTION

The ADDvantage-32 application software control scheme is based on control blocks. A control block is a software procedure which takes the inputs to the block, performs its function, and outputs the results. The following control blocks are not used in all software applications. They are a combination of all available control blocks. Refer to Appendix A for software specific control block interconnections.

### 4.1 2 AND

This block implements a 2 input digital AND gate.



FI

FIGURE 4-1. 2 AND BLOCK

#### 1. Inputs

INPA: Bit  
INPB: Bit

2.    Outputs

OUT:       Bit

3.    Implementation

OUT is set to one if both INPA and INPB are equal to one.

OUT is set to a zero bit if either INPA or INPB is equal to zero.



## 4.2 2 OR

This block implements a 2 input digital OR gate.

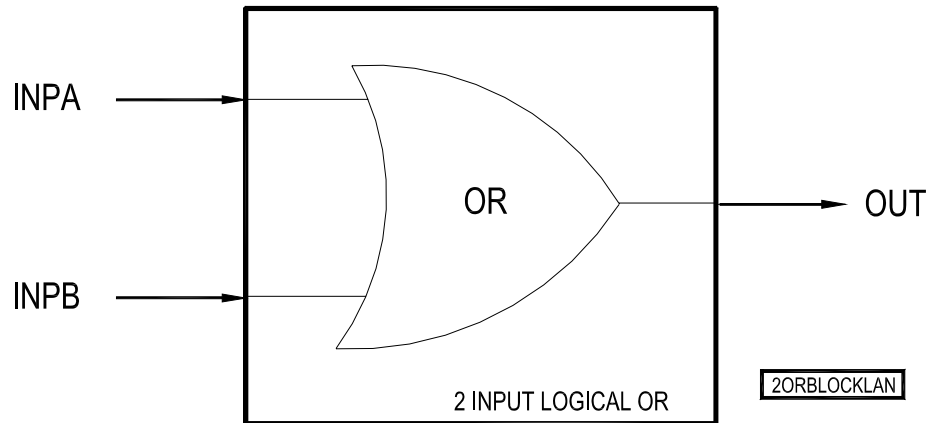


FIGURE 4-2. 2 OR BLOCK

### 1. Inputs

INPA: Bit  
INPB: Bit

### 2. Outputs

OUT: Bit

### 3. Implementation

OUT is set to one if either INPA or INPB is equal to one, else  $OUT = 0$ .

### 4.3 4 ANALOG SELECT

This block is used to select one of four possible analog signal paths. It can be used to control the application of multiple reference signals to a single input point.

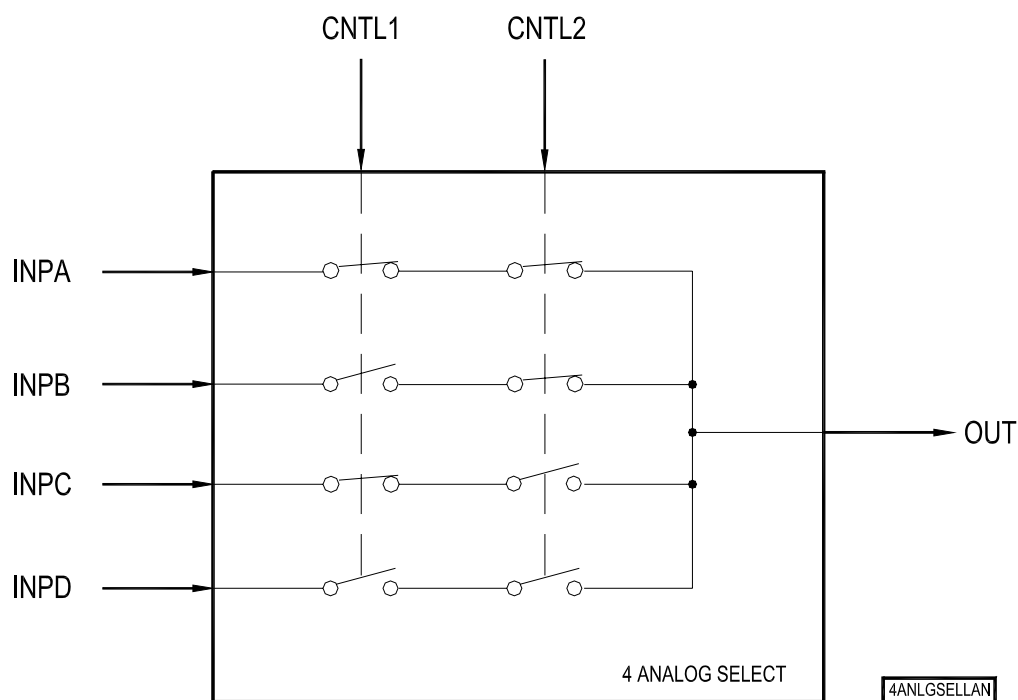


FIGURE 4-3. 4 ANALOG SELECT BLOCK

#### 1. Inputs

INPA: Analog  
 INPB: Analog  
 INPC: Analog  
 INPD: Analog

CNTL1: Bit  
 CNTL2: Bit

#### 2. Output

OUT: Analog

### 3. Implementation

One of the input signals will be directed to the block output by the following combinations of control bits.

CNTL1	CNTL2	OUT
0	0	INPA
1	0	INPC
0	1	INPB
1	1	INPD

#### 4.4 5 AND

This block implements a 5 input digital AND gate.

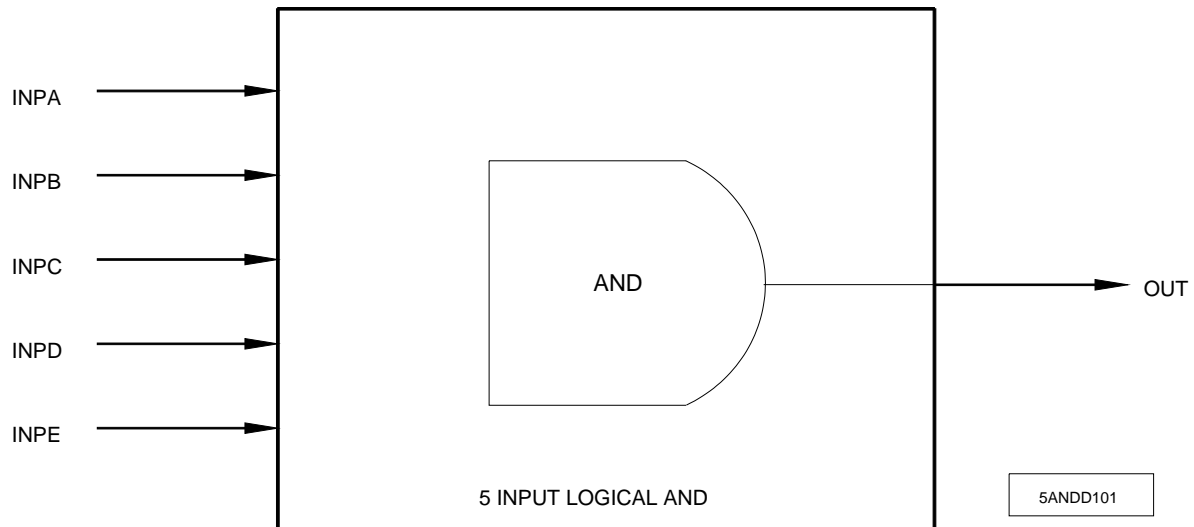


FIGURE 4-4. 5 AND BLOCK

1. Inputs

INPA: Bit  
INPB: Bit  
INPC: Bit  
INPD: Bit  
INPE: Bit

2. Outputs

OUT: Bit

3. Implementation

OUT = 1 if INPA, INPB, INPC, INPD, and INPE are equal to one.

OUT = 0 if any input is equal to zero.

## 4.5 5 SUMMER

The 5 Summer block selectively sums up to five analog input signals. The selection of which inputs are to be summed is set using a series of digital bits.

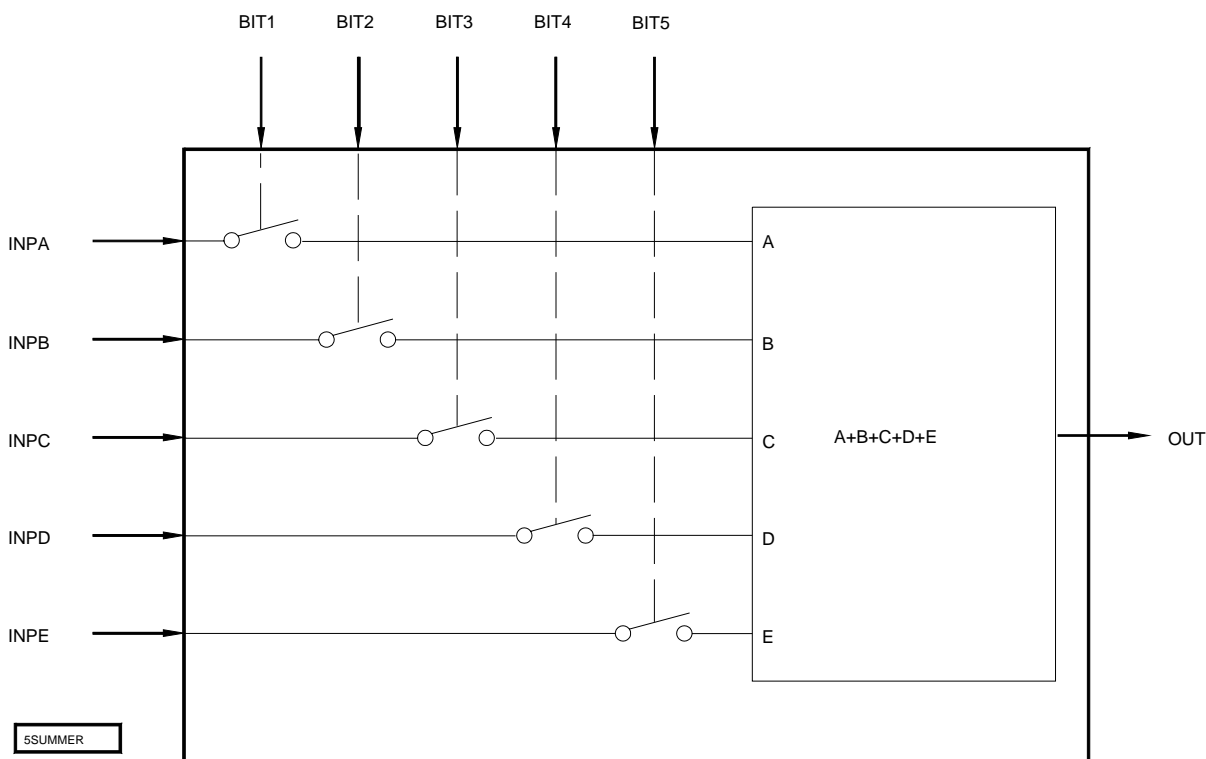


FIGURE 4-5. FIVE SUMMER BLOCK

### 1. Inputs

INPA: Analog  
 INPB: Analog  
 INPC: Analog  
 INPD: Analog  
 INPE: Analog  
 BIT1: Bit  
 BIT2: Bit  
 BIT3: Bit  
 BIT4: Bit  
 BIT5: Bit

### 2. Output

OUT: Analog

3. Implementation

$$\text{OUT} = (\text{INPA} \times \text{BIT1}) + (\text{INPB} \times \text{BIT2}) + (\text{INPC} \times \text{BIT3}) + (\text{INPD} \times \text{BIT4}) + (\text{INPE} \times \text{BIT5})$$

If all 5 bits are low, then  $\text{OUT} = 0$ .

## 4.6 8 BIT INVERT

The 8 BIT INVERT block takes the INP bit and the next seven and inverts them.

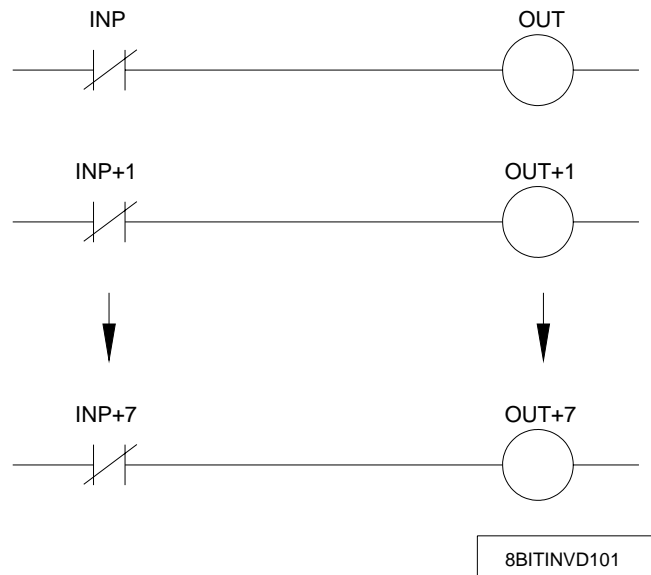


FIGURE 4-6. 8 BIT INVERT BLOCK

### 1. Inputs

INP: Digital

### 2. Outputs

OUT: Digital

### 3. Implementation

If INP is high (1), then OUT will be low (0).

If INP is low (0), then OUT will be high (1).

The same occurs for the next seven input bits. They are outputted to the next seven output addresses.

## 4.7 ABSOLUTE VALUE (ABS)

The Absolute Value block selectively takes the absolute value of an analog variable. The state of EN BIT determines if the OUT value equals INP or the absolute value of the INP value.

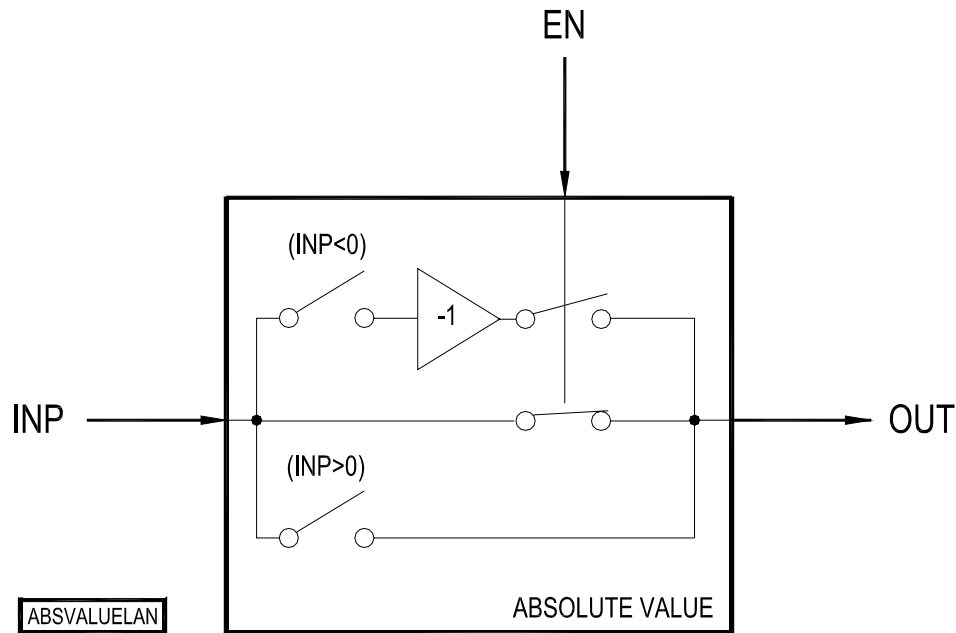


FIGURE 4-7. ABSOLUTE VALUE BLOCK

### 1. Inputs

INP:        Analog  
EN:        Bit

### 2. Output

OUT:        Analog

### 3. Implementation

If EN is low, then  $OUT = INP$ .

If EN is high, then  $OUT = \text{the absolute value of } INP$ .



## 4.8 ANALOG INVERT

The Invert block is used to invert the value of an analog signal.

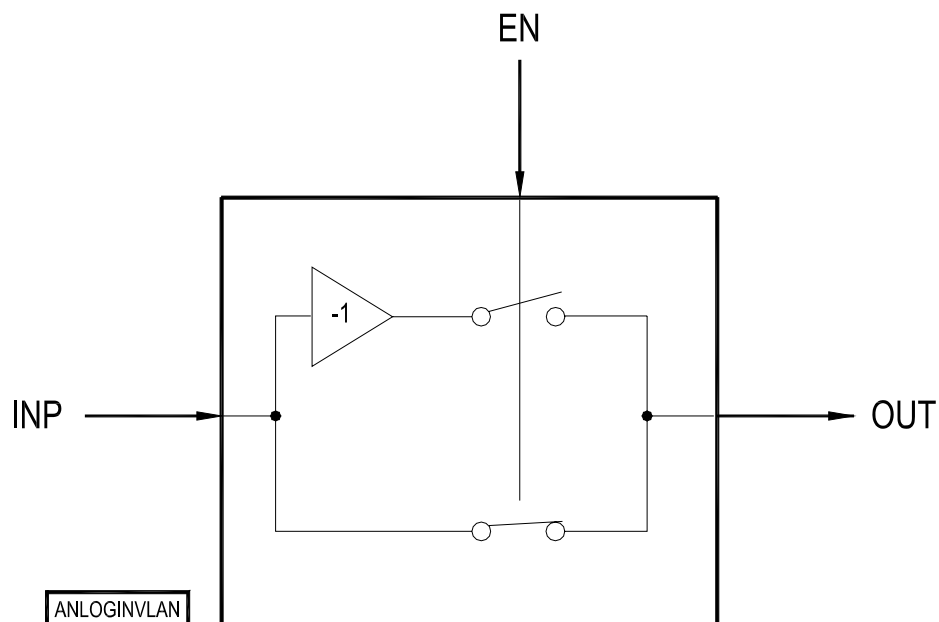


FIGURE 4-8. ANALOG INVERT BLOCK

### 1. Inputs

INP: Analog  
EN: Bit

### 2. Outputs

OUT: Analog

### 3. Implementation

If EN is low, then  $OUT = INP$ .

If EN is high, then  $OUT = -INP$ .

## 4.9 ANALOG SELECT

This block is used to select one of two different analog signal paths; for example, switching from field current reference to field economy reference.

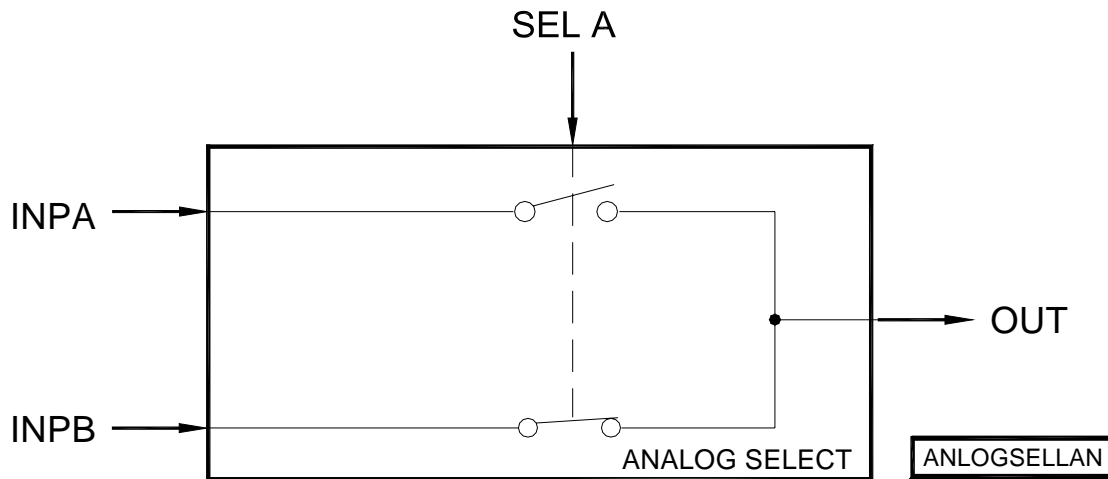


FIGURE 4-9. ANALOG SELECT BLOCK

### 1. Inputs

INPA: Analog  
INPB: Analog  
SELA: Bit

### 2. Outputs

OUT: Analog

### 3. Implementation

If SELA bit is high (set at 1), the OUTPUT is equal to INPA. If SELA bit is low (set at 0), the OUTPUT is equal to INPB.

## 4.10 ANALOG SWITCH

This block is used to switch in references to control the passage of an analog value or signal between control blocks.

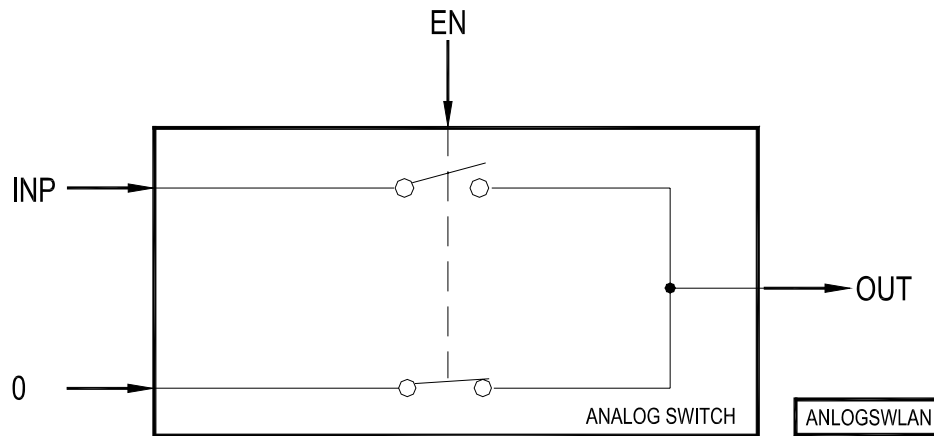


FIGURE 4-10. ANALOG SWITCH BLOCK

### 1. Inputs

INP:        Analog  
EN:        Bit

### 2. Outputs

OUT:        Analog

### 3. Implementation

If the EN bit is high, then OUT is equal to INP.  
If the EN bit is low, OUT is equal to zero.

## 4.11 ASM AUTO SHEET MARKER

This block sets an output bit high when the number of sheets cut equals an operator-entered setpoint (MARK STPT). The output bit also goes high when the number of sheets cut equals integer multiples of the setpoint. Therefore, every nth sheet sets the output bit high. The output bit remains high for the number of sheets entered in calibration as MARK HOLD; then the bit goes low. The internal counter resets when the MARK RESET bit is high.

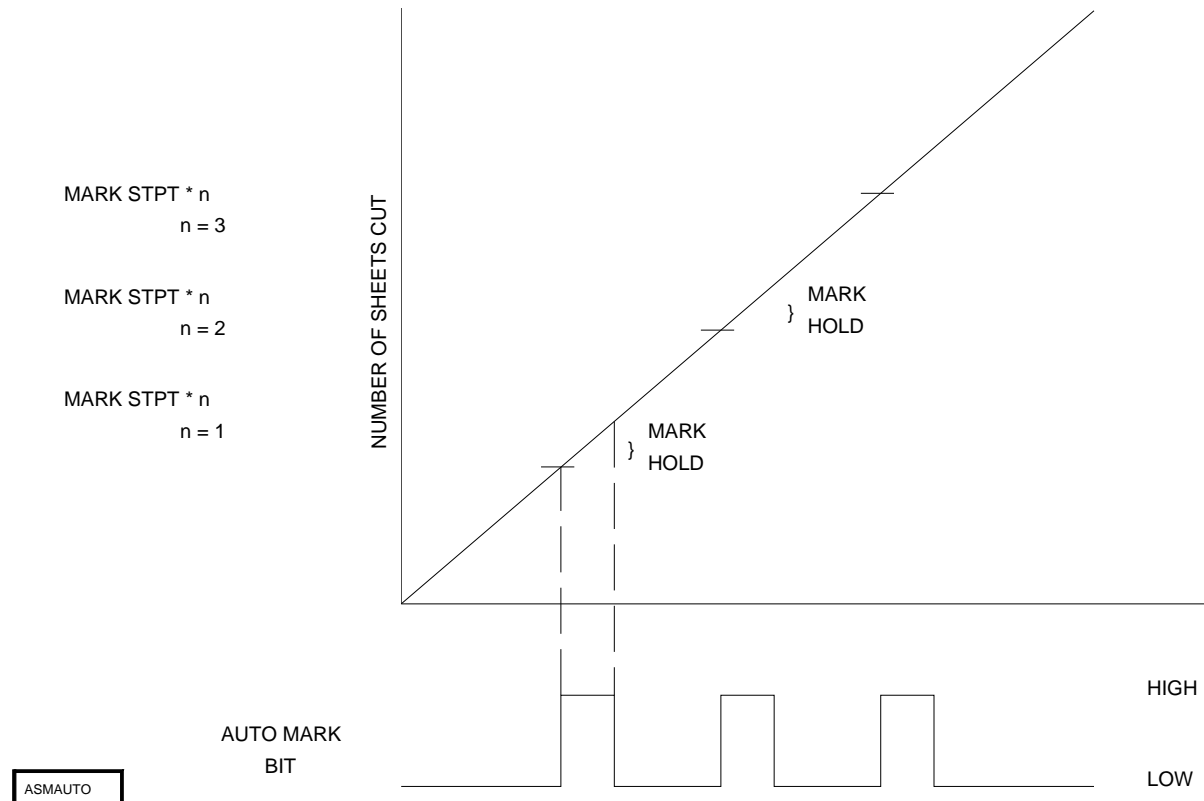


FIGURE 4-11. ASM AUTO SHEET MARKER BLOCK

### 1. Inputs

NUMBER SHTS:	Analog
MARK STPT:	Analog
MARK HOLD:	Analog
MARK RESET:	Bit

2.    Outputs

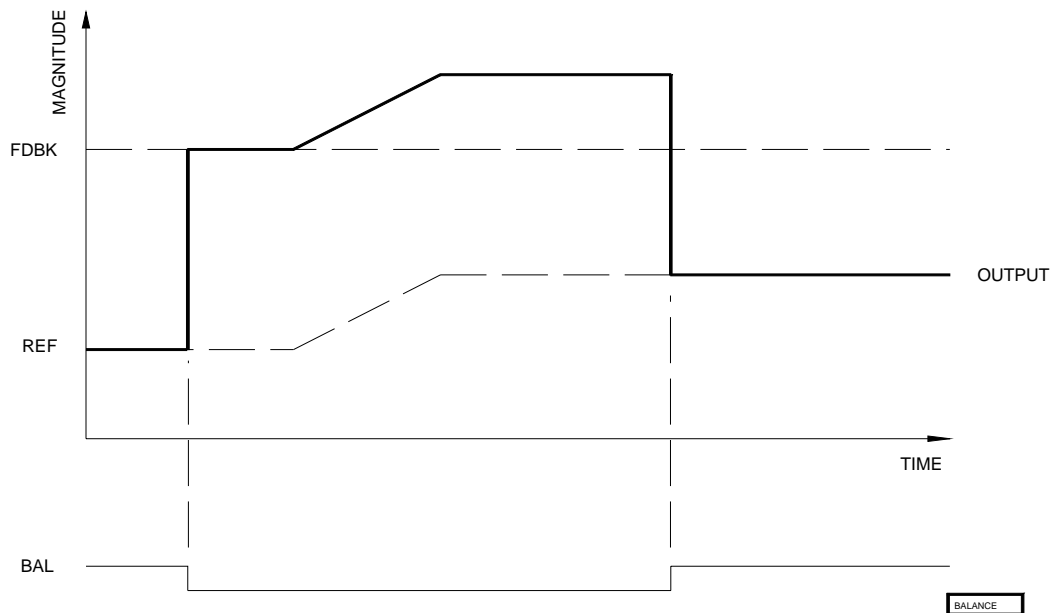
AUTO MARK:       Bit

3.    Implementation

If NUMBER SHTS = MARK STPT, then AUTO MARK goes high. If NUMBER SHTS = MARK STPT + MARK HOLD, then AUTO MARK goes low and  $n = n + 1$ . If MARK RESET bit is high, then  $n = 1$ .

## 4.12 BALANCE

The Balance block switches from one control scheme to another without changing the current operating reference.



FIG

URE 4-12. BALANCE BLOCK

### 1. Inputs

REF: Analog  
 FDBK: Analog  
 BAL: Bit  
 RET: Bit

### 2. Outputs

OUT: Analog  
 DIF: Analog

### 3. Implementation

On a falling edge of the BAL input, DIF will be sampled as REF-FDBK. "DIF" will not change until the next falling edge of the BAL input.

When the BAL input is low,  $OUT = REF - DIF$ .

When the BAL input is high,  $OUT = REF$ .

Non-retentive Block

On powerup of the ADDvantage-32, "err"=0.

Retentive Block

On powerup of the ADDvantage-32, DIF will be initialized under the following conditions:

If  $RET = 0$ ,  $DIF = 0$ .

If  $RET = 1$ , DIF is set to its last value. DIF must also be configured to a retentive point (Y\*\*\*:RET SETPT\*) to be updated automatically on powerup.

### 4.13 BIT CONVERT

The Bit Convert block converts 4 input bits into decimal numbers. The output changes only when the ENABLE bit is high. This block can also be used as the X\_IN value of a Table block enabling 16 separate setpoints.

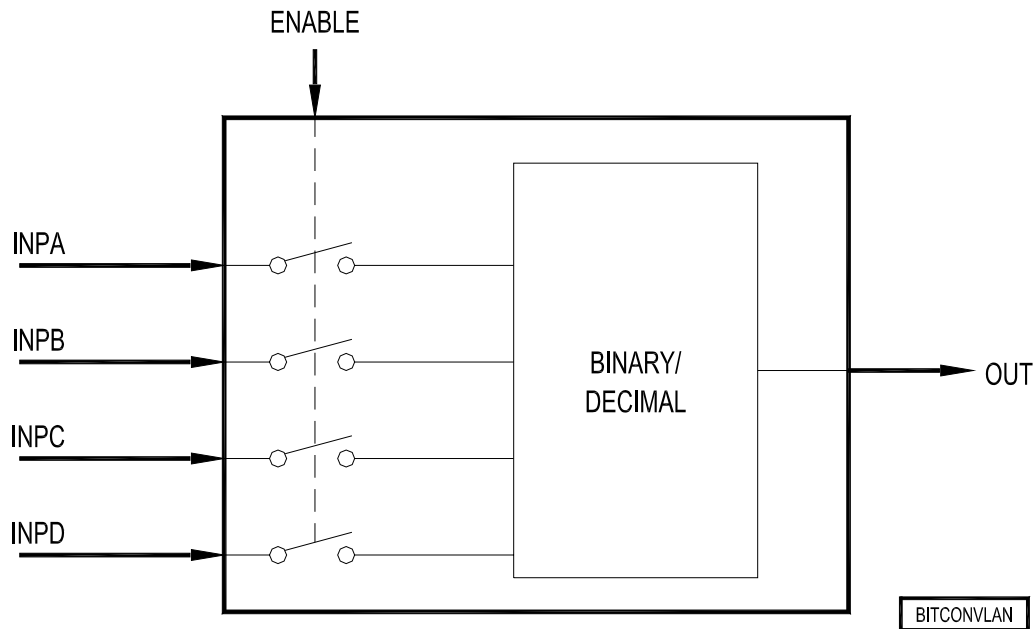


FIGURE 4-13. BIT CONVERT BLOCK

#### 1. Inputs

INPA: Bit  
 INPB: Bit  
 INPC: Bit  
 INPD: Bit  
 ENABLE: Bit

#### 2. Outputs

OUT: Analog

#### 3. Implementation

OUT latches only when the ENABLE input is low. OUT defaults to 0 on powerup.

When the ENABLE bit is high, refer to the following table to determine the value of OUT.



TABLE 4-13. Bit Convert Block OUT Values

INPA	INPB	INPC	INPD	OUT
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	15

#### 4.14 BIT INVERT

A Bit Invert block is used to provide an output bit which is always the opposite state of the blocks input bit.

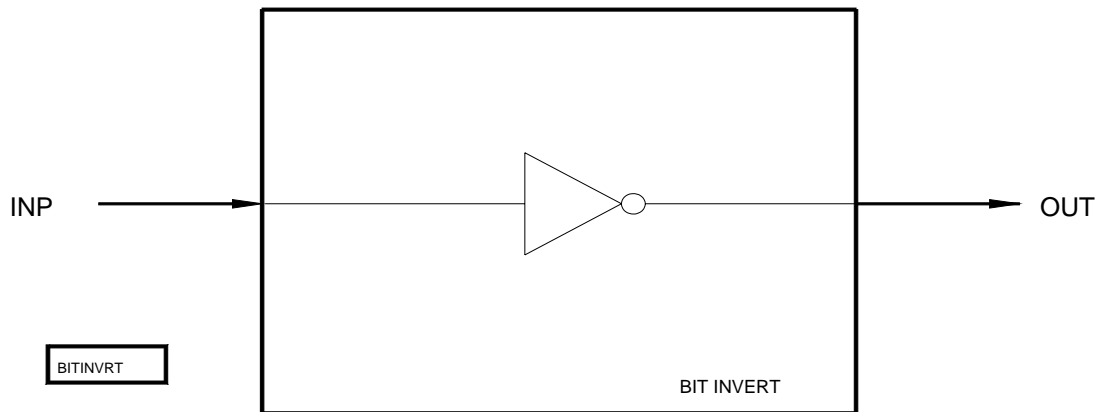


FIGURE 4-14. BIT INVERT BLOCK

1. Inputs

INP: Bit

2. Outputs

OUT: Bit

3. Implementation

If INP bit is high, OUT bit is set low.

If INP bit is low, OUT bit is set high.

#### 4.15 BIT SELECT

This block is used to select one of two different bit signal paths.

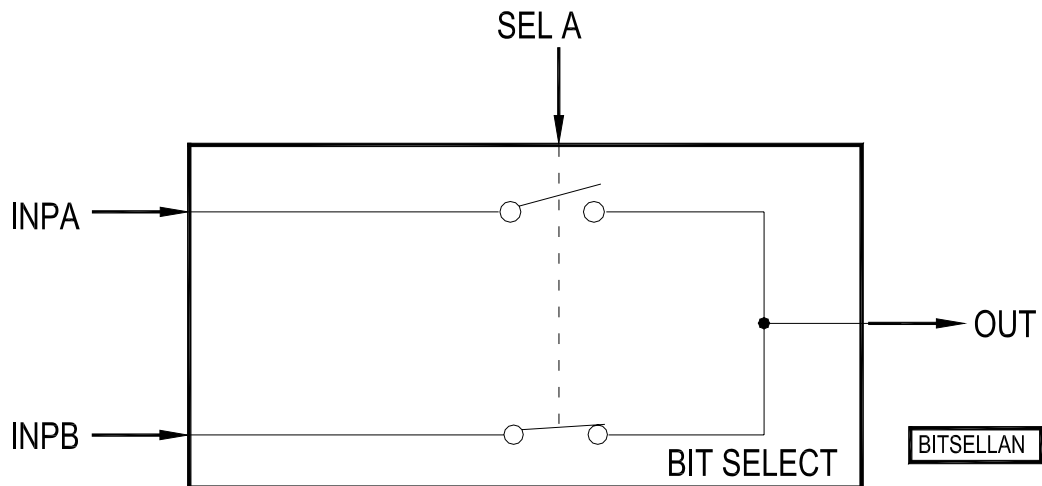


FIGURE 4-15. BIT SELECT BLOCK

1. Inputs

INPA: Bit  
INPB: Bit  
SEL A: Bit

2. Outputs

OUT: Analog

3. Implementation

If SEL A bit is high (set at 1), OUT is equal to INPA.  
If SEL A bit is low (set at 0), OUT is equal to INPB.

## 4.16 BUMPLESS SWITCH

This block is used to provide a smooth "BUMPLESS" transition when switching control, reference, or feedback between two analog signals.

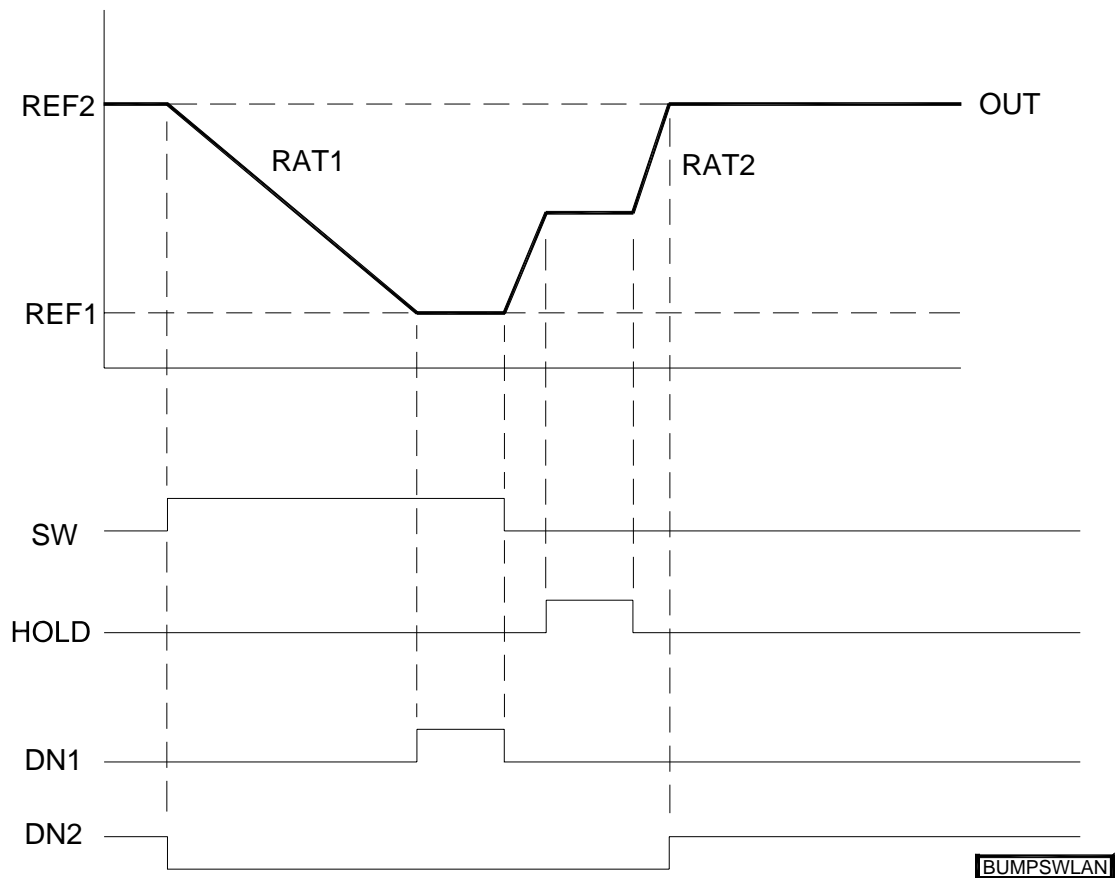


FIGURE 4-16. BUMPLESS SWITCH BLOCK

### 1. Inputs

REF1:	Analog
REF2:	Analog
RAT1:	Analog
RAT2:	Analog
SW:	Bit
HOLD:	Bit

## 2. Outputs

OUT:            Analog  
DN1:           Bit  
DN2:           Bit

## 3. Implementation

The RAT1 input is the rate in units/second that the transfer takes place when switching from REF2 to REF1. RAT2 is the rate used when switching from REF1 to REF2. If the rate input = 0, the transfer is performed without ramping.

When SW goes high, the OUT ramps from REF2 to REF1 until OUT equals REF1, or when REF1 - REF2 polarity switches from the starting polarity. When this condition occurs, the DN1 bit goes high and the OUT follows REF1 without ramping.

When SW goes low, the OUT ramps from REF1 to REF2 in the same manner as previously described. When OUT equals REF2, the DN2 bit goes high and the OUT follows REF2 without ramping.

When the HOLD bit goes high, the OUT freezes at the current value. When deactivated, the OUT ramps using the associated rate value to the input value selected by SW. If the appropriate DONE BIT was set, it will be cleared at the removal of the hold bit until the ramping is complete.

#### 4.17 CDS COUNTS DURING STOP

This block calculates the number of pulses that will be counted during a controlled stop. It is used in turret applications to determine when the drive run should be removed so that the turret will stop at the appropriate index position.

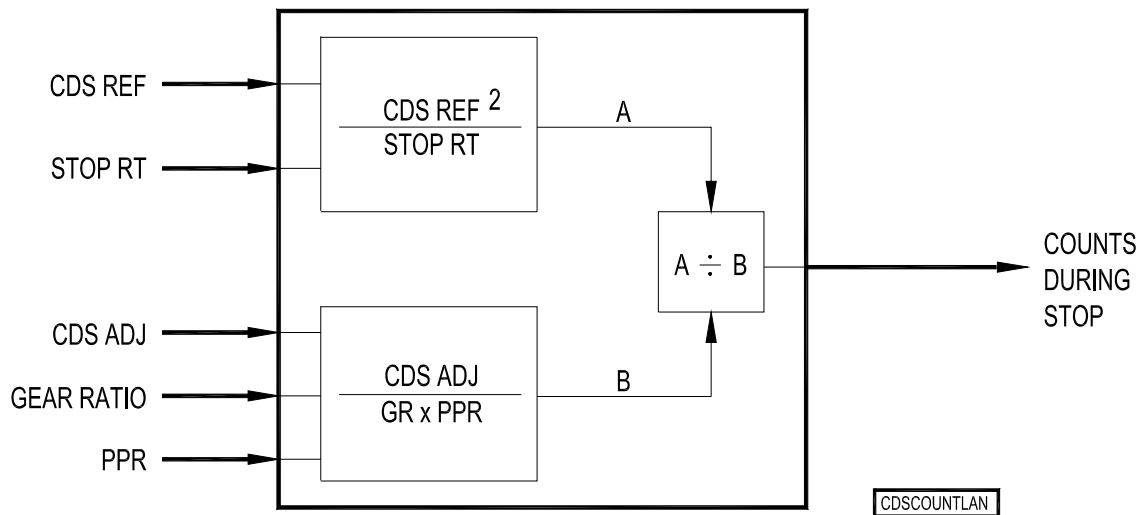


FIGURE 4-17. CDS COUNTS DURING STOP BLOCK

##### 1. Inputs

CDS REF:	Analog
STOP RT:	Analog
CDS ADJ:	Analog
GEAR RATIO:	Analog
PPR:	Analog

##### 2. Outputs

COUNT STOP:	Analog
-------------	--------

3. Implementation

$$\text{CDS} = \frac{\frac{(\text{CDS REF})^2}{\text{STOPPING RT}}}{\frac{\text{CDS ADJ}}{\text{GR} \cdot \text{PPR}}} = \frac{(\text{CDS REF})^2 \cdot \text{GR} \cdot \text{PPR}}{\text{STOPPING RT} \cdot \text{CDS ADJ}}$$

Where:

CDS REF = REFERENCE IN RPM  
STOPPING RT = RATE IN RPM/SEC  
CDS ADJ =  $2 \times 60$  SEC/MIN  
GEAR RATIO = NO UNITS  
PPR = PULSES/REV

## 4.18 CLAMPING

A Clamping block is used to restrict an analog signal to a value between user selectable high (MAXL) and low (MINL) limits.

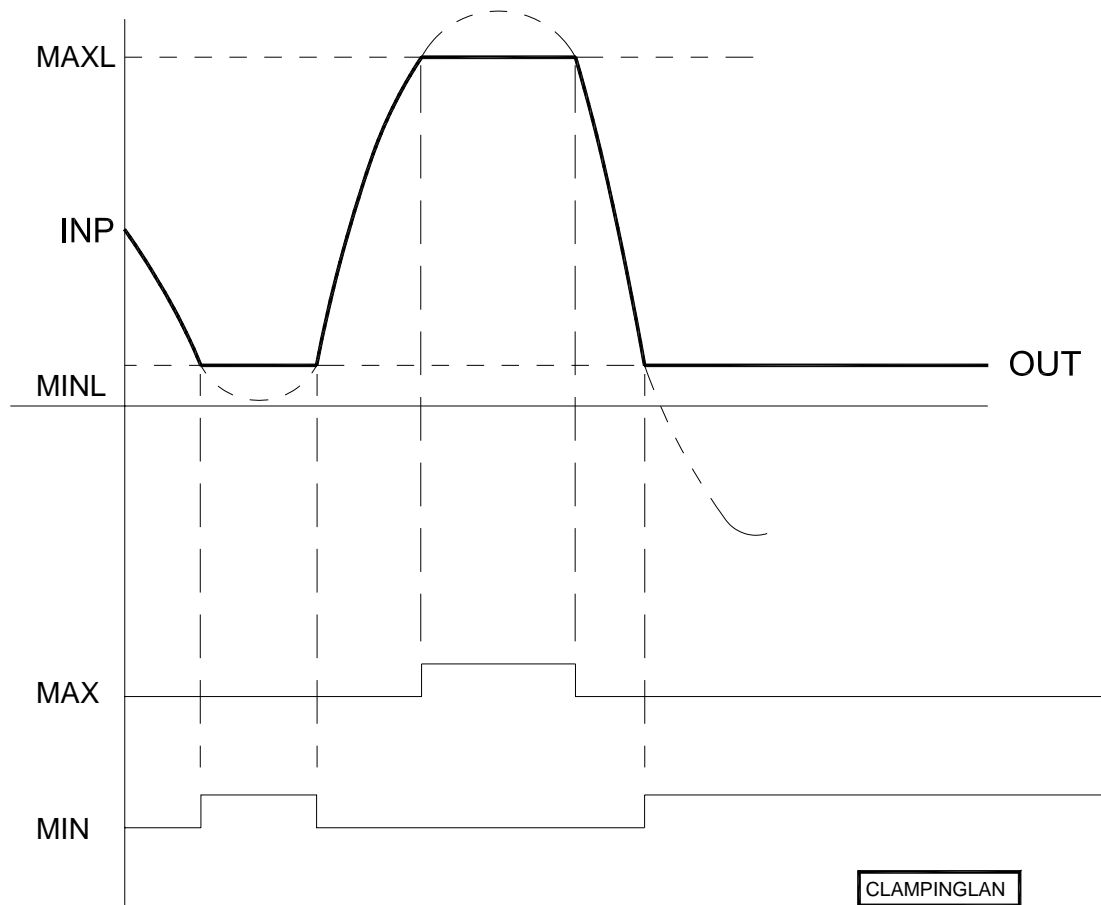


FIGURE 4-18. CLAMPING BLOCK

### 1. Inputs

INP: Analog  
 MAXL: Analog  
 MINL: Analog

### 2. Outputs

OUT: Analog  
 MAX: Bit  
 MIN: Bit



3. Implementation

If  $INP > MAXL$ , then  
     $OUT = MAXL$   
     $MAX = \text{high}$ ,  $MIN = \text{low}$

If  $INP < MINL$ , then  
     $OUT = MINL$   
     $MIN = \text{high}$ ,  $MAX = \text{low}$

If  $MINL < INP < MAXL$ , then  
     $OUT = INP$   
     $MAX = \text{low}$   
     $MIN = \text{low}$

## 4.19 COM LOSS

The Com Loss block is used as a communication watchdog.

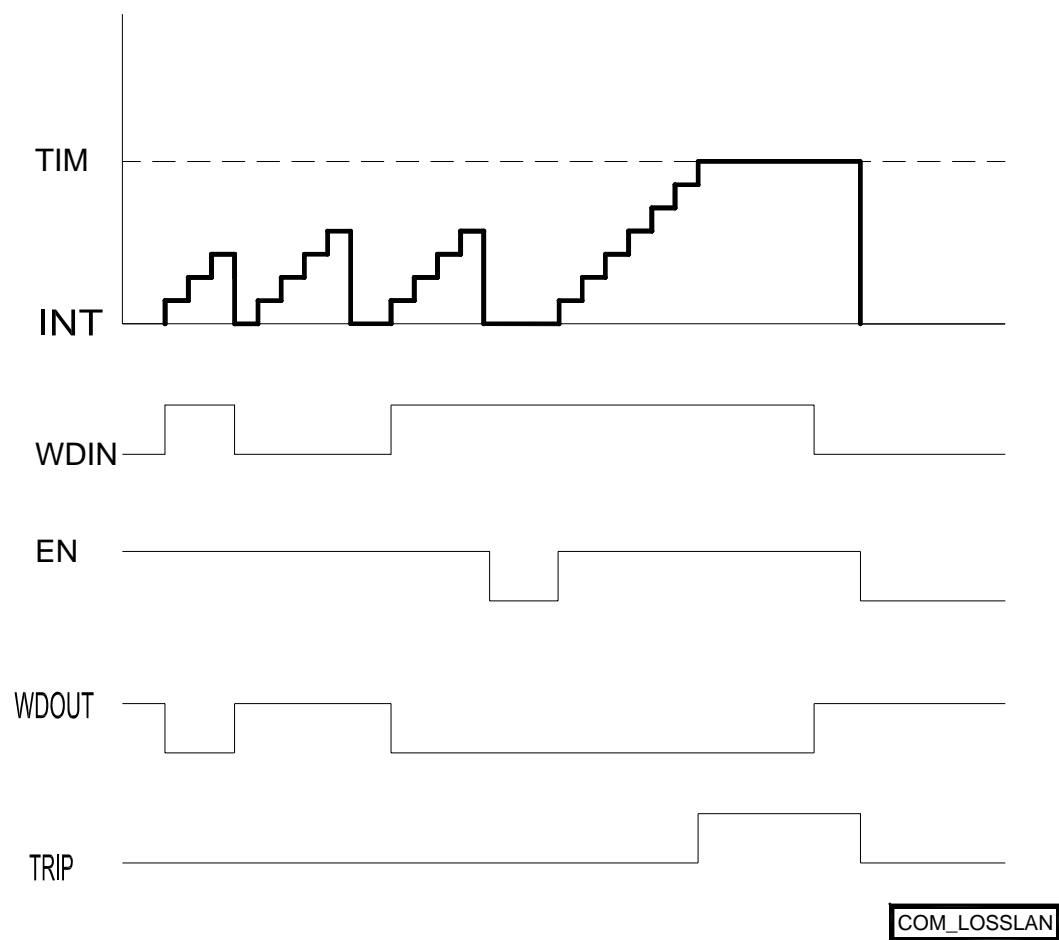


FIGURE 4-19. COM LOSS

### 1. Inputs

TIM:	Bit
EN:	Bit
WDIN:	Bit

### 2. Outputs

WDOUT:	Bit
TRIP:	Bit

## 4.20 COM WD

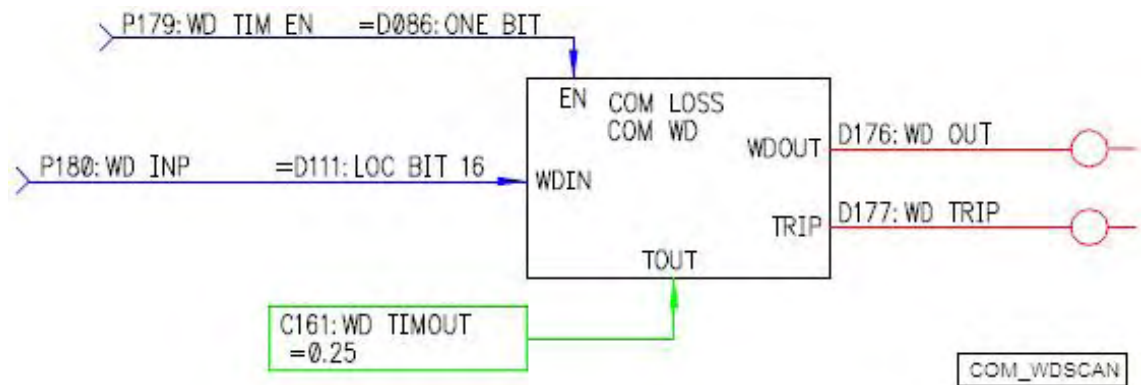


FIGURE 4-20. COM WD BLOCK

### 1. Inputs

EN:	Bit
WD IP:	Bit
TOUT:	Analog

### 2. Outputs

WDOUT	Bit
TRIP	Bit

### 3. Implementation

When the EN input of the WD COM block is a logic level high (One Bit), the block monitors the WDIN input and will set the TRIP output if the input fails to toggle (transition from low to high or transition from high to low) within the time period (seconds) defined by the TOUT input. The WD OUT bit equates to the bit inverted state of the WDIN input. The TRIP output will be reset to a logic level low (Zero Bit) when the EN input is set to a logic level low signal or if the WDIN begins to toggle at a rate greater than the TOUT time period.

## 4.21 COMPARATOR

Use this block to set an output bit when the input is greater than a setpoint. The HYS input sets up hysteresis to debounce the output bit.

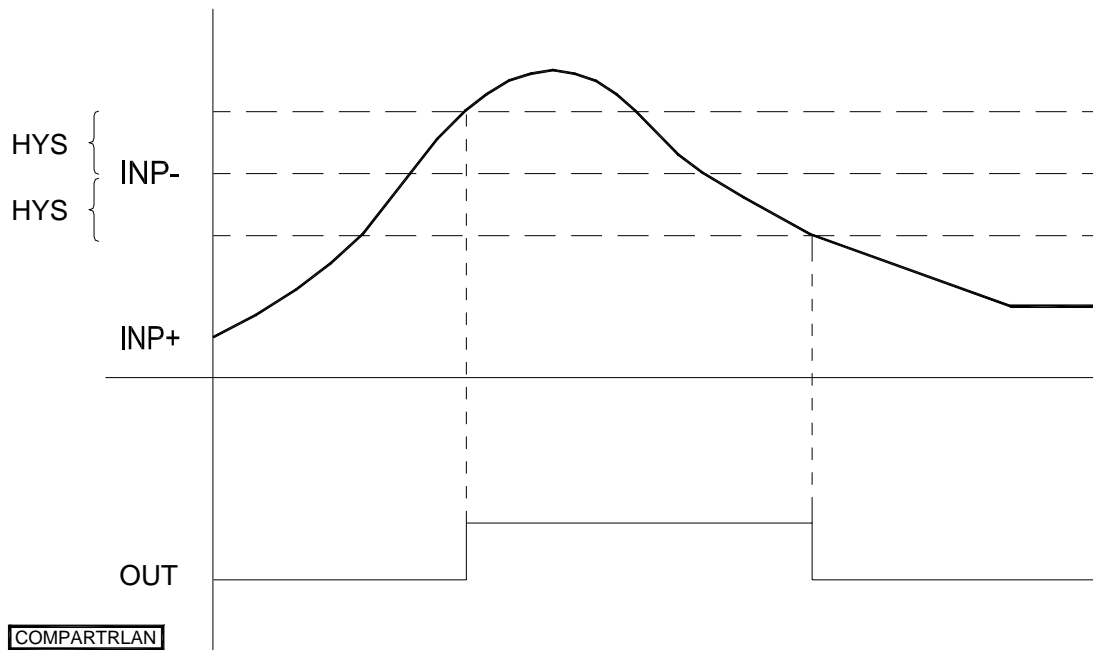


FIGURE 4-21. COMPARATOR BLOCK

### 1. Inputs

INP+: Analog  
 INP-: Analog  
 HYS : Analog

### 2. Outputs

OUT: Bit

### 3. Implementation

If INP+ increases so:  $INP+ - HYS > INP-$  then the OUT bit will go high.

If INP+ decreases so:  $INP+ + HYS \leq INP-$  then the OUT bit will go low.

## 4.22 COPY

The Copy block takes the analog value at the input and copies the value to the output.

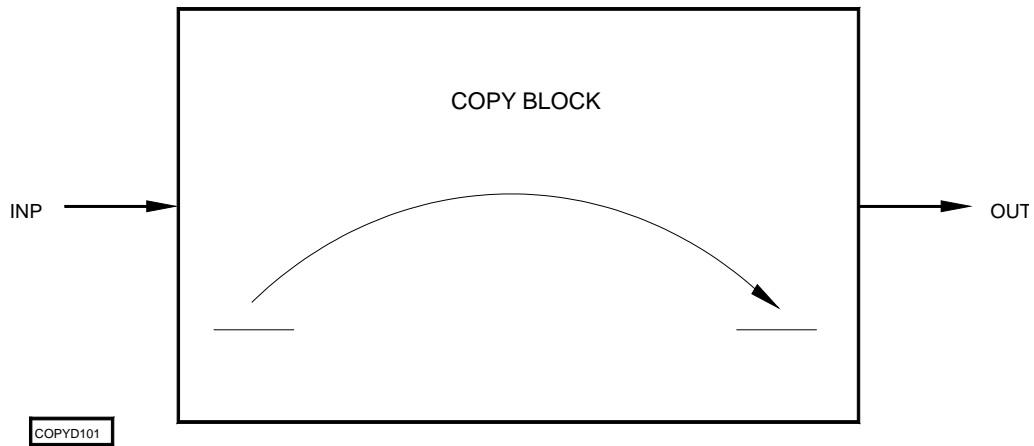


FIGURE 4-22. COPY BLOCK

### 1. Inputs

INP: Analog

### 2. Outputs

OUT: Analog

### 3. Implementation

$OUT = INP$

## 4.23 CURRENT LIMIT

This block provides the user with a feature for selecting an automatic taper back of the drive current limits by two events or using fixed current limits.

The first event, if enabled by P\*\*\*:BYPASS I2R = ZERO BIT (DEFAULT), prevents the drive from faulting on a MOTOR (II) T fault. The current limit block accomplishes this by lowering the current limit when A\*\*\*:IIR INTEGR is  $\geq$  to 25 counts. The MOTOR (II) T fault indicates a motor thermal overload condition where the motor armature current was above 100% for more than the time specified by X\*\*\*:Thermal TC.

The motor will be allowed to operate at 150% armature current for 60 seconds if the Thermal TC is set to 60.0 (DEFAULT). The motor could operate up to 200% armature current, but the MOTOR (II) T fault would occur much sooner than 60 seconds. The user can increase the Thermal TC value up to a maximum of 3,000 seconds.

The drive will fault on a BRDGE (II) T fault when drive armature current is 150% of the drive D.C. MAX CONT nameplate current for 60 seconds. This is an Underwriters Laboratories (UL) mandated fault where the magnitude and time cannot be altered by users.

When actual motor armature current rises above 110% motor nameplate, IIR INTEGR will count up from zero when current is rising and count down when current falls below 110%. The IIR INTEGR is used to calculate motor temperature. The rate at which IIR INTEGR counts is determined by the magnitude of armature current above 100% and the thermal TC value.

The current limit taper feature can be disabled by setting P\*\*\*:BYPASS I2R = ONE BIT. In this nontaper mode, IIR INTEGR will continue counting when motor armature current is above 110% until it reaches the maximum count of 100 and faults the drive on a MOTOR (II) T fault.

The second event provides automatic taper back of the drive current limit to prevent commutation faults due to overcurrenting the armature above base speed. The current limit should be set below 150% at maximum motor speed to prevent flashovers.

The user can configure the motor current limits using parameters P\*\*\*:MAX I LIMIT and P\*\*\*:MIN I LIMIT. These parameters are defaulted to C\*\*\*:POS CUR LMT = 100 and C\*\*\*:NEG CUR LMT = 100 respectively. The user can enter different current limits by entering a new value for the "C" parameter corresponding to the POS CUR LMT or NEG CUR LMT. The value is entered as a percentage of the motor nameplate armature current. It is assumed the user has correctly scaled the motor armature current to the drive D.C. MAX CONT nameplate current by setting X\*\*\*:MOTOR IARM.

Regardless of the POS I LIMIT or NEG I LIMIT values for the motor current limits, actual armature current cannot exceed 200% of the drive D.C. MAX CONT nameplate current.

### 1. Inputs

POS I:	Analog	0 - 300
NEG I:	Analog	0 - 300
START PER:	Analog	100 - 200
END PER:	Analog	0 - 200
I2R TRIP:	Analog	0 - 100
BY I2R:	Bit	
SFDBK:	Analog	
START PER S:	Analog	0 - 200
END PER S:	Analog	0 - 200
BRK SPD:	Analog	
MAX SPD:	Analog	
BLOCK POS:	Bit	
BLOCK NEG:	Bit	

### 2. Outputs

POS LIM:	Analog	0 - 200
NEG LIM:	Analog	0 - 200

### 3. Implementation

The Current Limit block emulates the block diagram in Figure 4-21.

The POS I LIMIT and NEG I LIMIT outputs are usually configured to the MAXL and MINL inputs on the speed loop PI Control block.

#### Non-Tapered Current Limits

If non-tapered current limits are desired, the BY I2R input must be high by configuring P\*\*\*:BYPASS I2R = ONE BIT. The current limit block constantly monitors the I2R Trip input (A\*\*\*:IIR INTEGR) to detect when the motor armature current rises above 110%. The IIR INTEGR value will count up as long as the current is above 110%. Should the armature current fall below 110%, the IIR INTEGR will count down. IF the armature current stays above 110% long enough for IIR INTEGR to accumulate 100 counts, the drive will fault on a MOTOR (II) T fault.

The POS I LIMIT and NEG I LIMIT outputs will equal the POS I and NEG I input values respectively.

### Tapered Current Limits

If tapered current limits are desired, the BY I2R input must be low by configuring P\*\*\*:BYPASS I2R = ZERO BIT. The current limit block constantly monitors the I2R Trip input (A\*\*\*:IIR INTEGR) to detect when the motor armature current rises above 110%. A hidden I2R Trip table is created within the current limit block to limit the POS LIM and NEG LIM outputs when the motor armature current rises above 110%. The POS LIM and NEG LIM outputs will equal the smaller value of either the table output or the POS I and NEG I inputs. The table output will equal the START PER (C\*\*\*:START PER S) when IIR INTEGR < 25 counts. When IIR INTEGR = 100 counts, the table output will equal END PER (C\*\*\*:END PER S) where the user should enter a value of 100% or less. When IIR INTEGR is between 25 to 100 counts, the table output is equal to the interpolation between START PER and END PER.

The POS LIM and NEG LIM outputs are then checked against another hidden SFDBK table within the block to check the current limits by the SFDBK input (A\*\*\*:ABS ACT SPD).

When SFDBK < BRK SPD, the speed table output will equal START PER S. IF SFDBK > MAX SPD, the speed table output will equal END PER S where the user should enter a value of 100% or less. When SFDBK is between BRK SPD and MAX SPD, the speed table output will equal the interpolation between START PER S and END PER S. The POS LIM and NEG LIM outputs will equal the smaller value of either the table output or the POS I and NEG I inputs.

### Block Positive Bridge

The Positive Bridge can be blocked by making the BLOCK POS input high by configuring P\*\*\*:BLOCK POS B = ONE BIT. The POS LIM output will equal zero when BLOCK POS is set high.

If BLOCK POS is set low (zero bit), POS LIM output will equal the smallest value between POS I input, the output of the I2R Trip table or the SFDBK table.

### Block Negative Bridge

The Negative Bridge can be blocked by making the BLOCK NEG input high by configuring P\*\*\*:BLOCK NEG B = ONE BIT. The NEG LIM output will equal zero when BLOCK NEG is set high.

If BLOCK NEG is set low (zero bit), NEG LIM output will equal the negative of the smallest value between NEG I input, the output of the I2R Trip table or the SFDBK table.



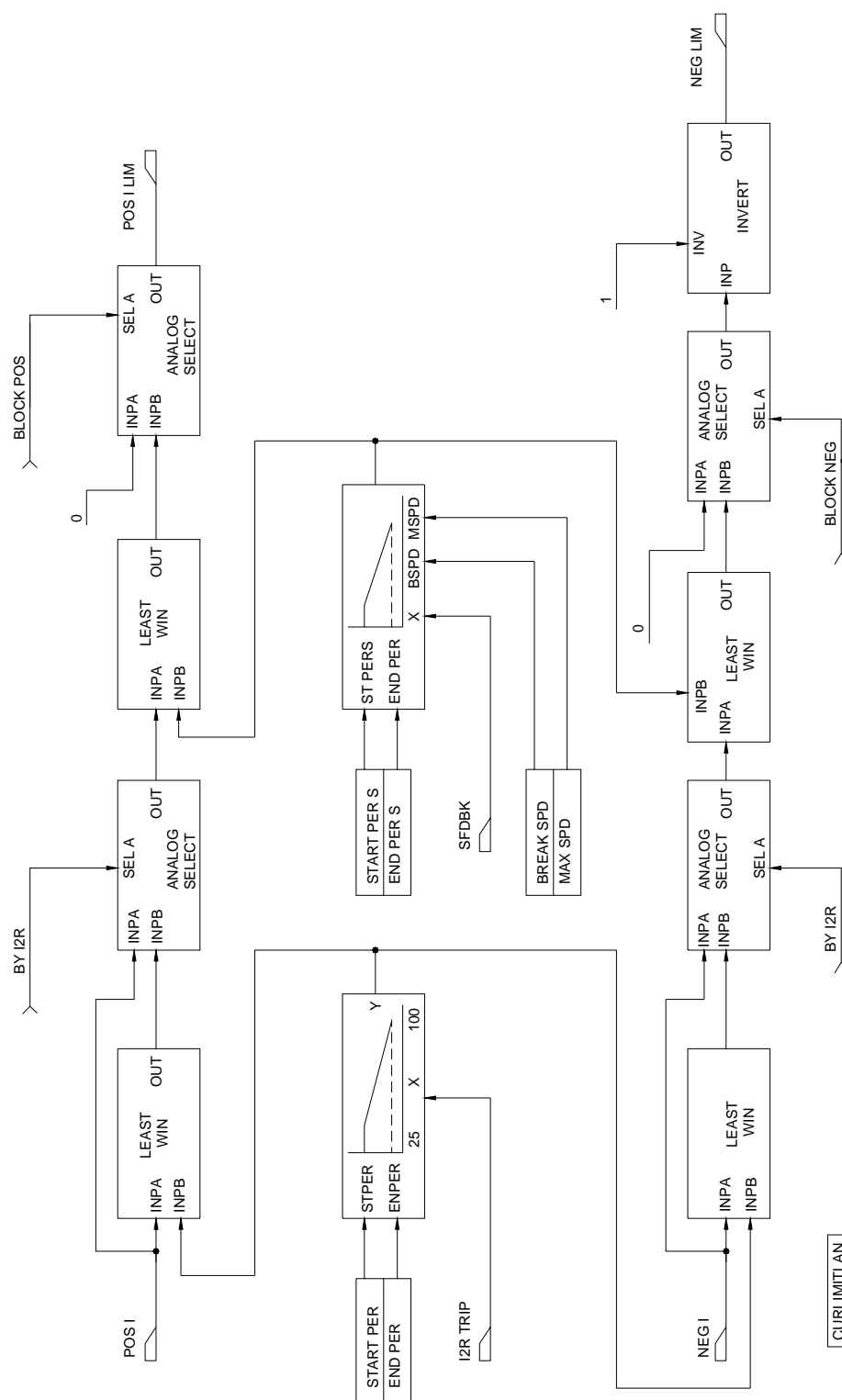


FIGURE 4-23. CURRENT LIMIT BLOCK DIAGRAM

## 4.24 DEADBAND

A Deadband block is used to reset an analog signal to zero when it is less than a user selected value.

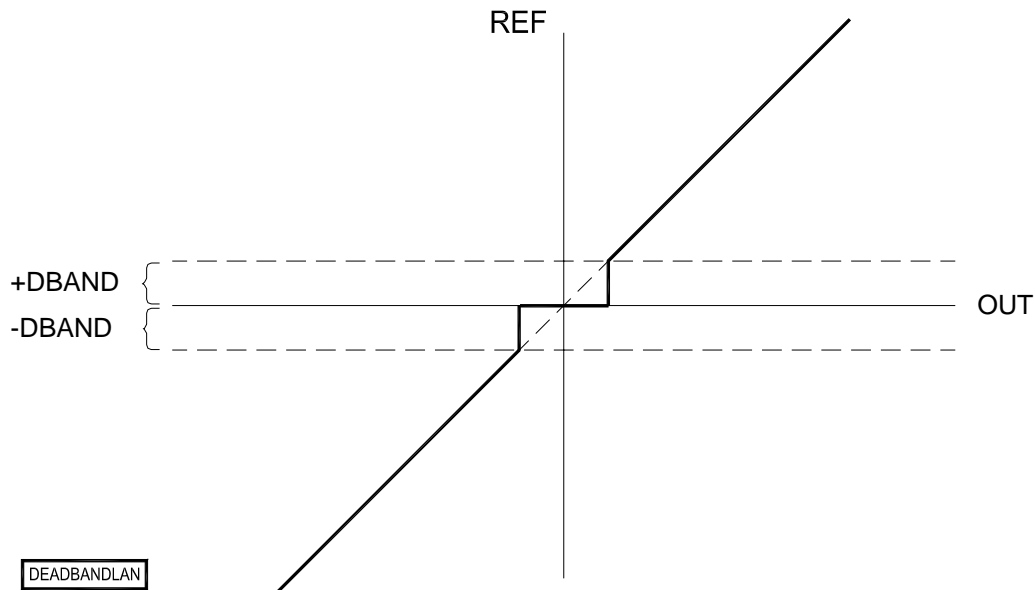


FIGURE 4-24. DEADBAND BLOCK

### 1. Inputs

REF: Analog  
DBAND: Analog

### 2. Outputs

OUT: Analog

### 3. Implementation

If  $-DBAND < REF < DBAND$  then  
     $OUT = 0$   
    else  
     $OUT = REF$

## 4.25 DEMUX

### 1. Inputs

BIT1: Bit  
BIT2: Bit  
INP: Bit

### 2. Outputs

OUT0 Bit  
OUT1 Bit  
OUT2 Bit  
OUT3 Bit

### 3. Implementation

The output bits are set as follows:

If BIT1 = 0 and BIT2 = 0 and INP = 1 then OUT0 = 1,  
else OUT0 = 0

If BIT1 = 1 and BIT2 = 0 and INP = 1 then OUT1 = 1,  
else OUT1 = 0

If BIT1 = 0 and BIT2 = 1 and INP = 1 then OUT2 = 1,  
else OUT2 = 0

If BIT1 = 1 and BIT2 = 1 and INP = 1 then OUT3 = 1,  
else OUT3 = 0

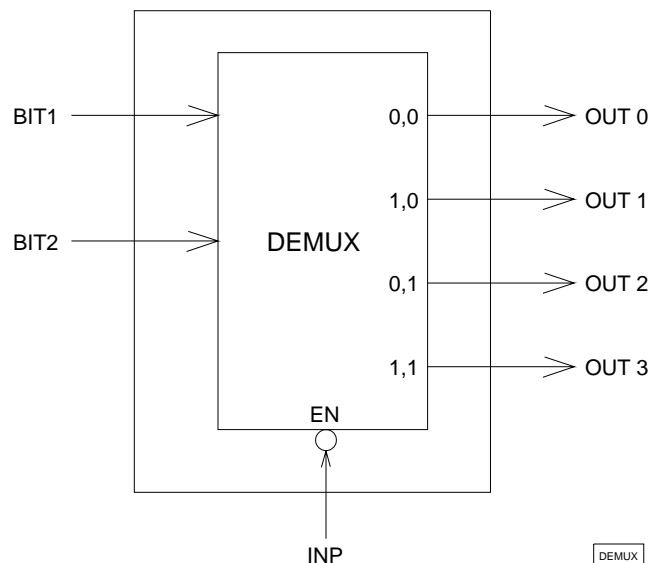


FIGURE 4-25. DEMUX BLOCK

## 4.26 DENSITY

This block is used to calculate the approximate density of a winding or unwinding reel of product. It calculates the density of a roll over specific diameter ranges. The range needs to be large enough to make the calculation accurately, taking into account error in the diameter measurements.

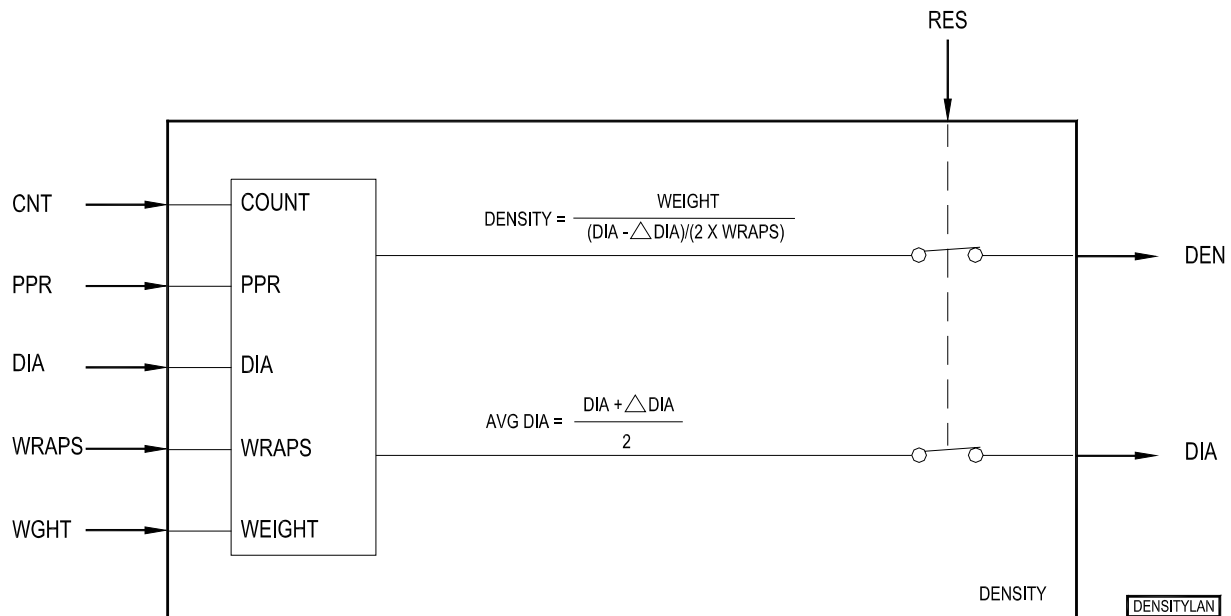


FIGURE 4-26. DENSITY BLOCK

### 1. Inputs

CNT:	Analog
PPR:	Analog
DIA:	Analog
WRAPS:	Analog
WGHT:	Analog
RES:	Bit

### 2. Outputs

DENSITY:	Analog
AVG DIA:	Analog

### 3. Implementation

When RES is high or on power up, the outputs = 0.

When not RES, the following occurs:

The outputs do not change until the number of winder revolutions equals WRAPS. (1 winder revolution = PPR amount of change in the CNT value) When this occurs, the following calculations are done.

$$\begin{aligned} \text{DIA} &= \text{DIA at start of wraps count} \\ \text{thick} &= (\text{DIA} - \text{DIA}) / (2 \times \text{WRAPS}) \\ \text{DEN} &= (\text{WGHT} / \text{thick}) \\ \text{ADIA} &= (\text{DIA} + \text{DIA}) / 2 \end{aligned}$$

The outputs do not change until the next time the number of winder evolutions equals WRAPS or a RES occurs.

## 4.27 DERIVATIVE GAIN (D/DT)

The D/DT block performs a derivative gain function. It can be used for inertia compensation.

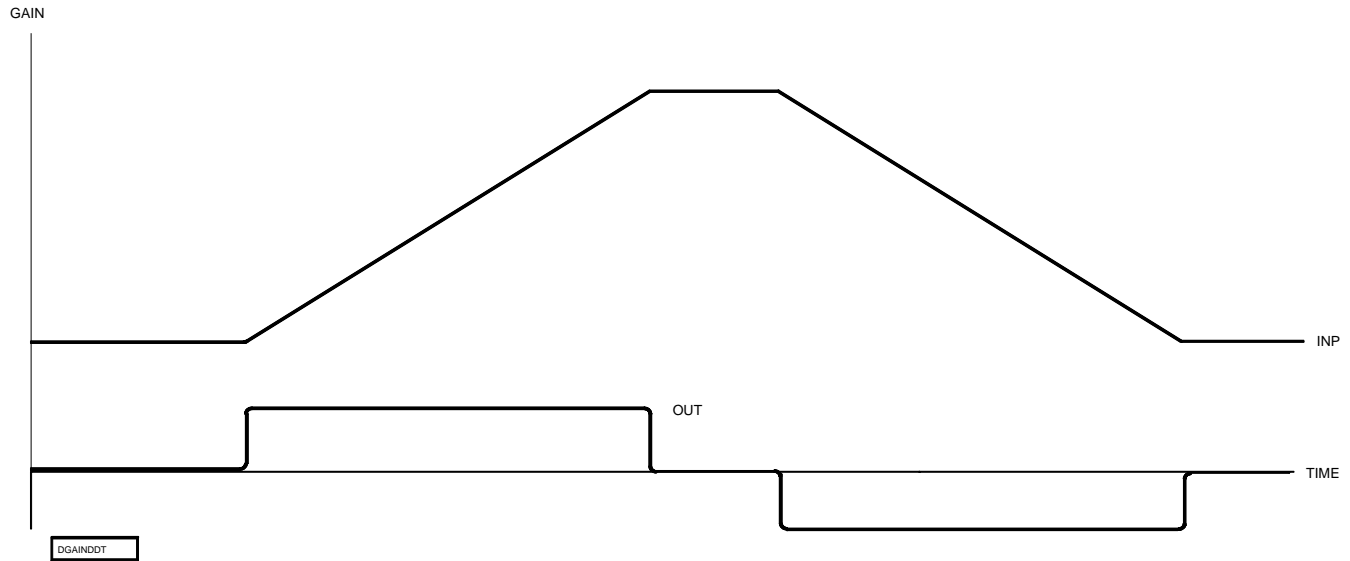


FIGURE 4-27. DERIVATIVE GAIN BLOCK

### 1. Inputs

INP: Analog  
GAIN: Analog  
LP: Analog

### 2. Outputs

OUT: Analog

### 3. Implementation

INP goes through a third order low pass filter with time constant LP in seconds. This filters amplification of high frequency bounce.

$$\text{OUT} = (\text{Rate of change of filtered INP}) \times \text{GAIN}$$

## 4.28 DIFF TRIP

This block is a combination differential comparator and timer. It is used to detect alarm or fault conditions.

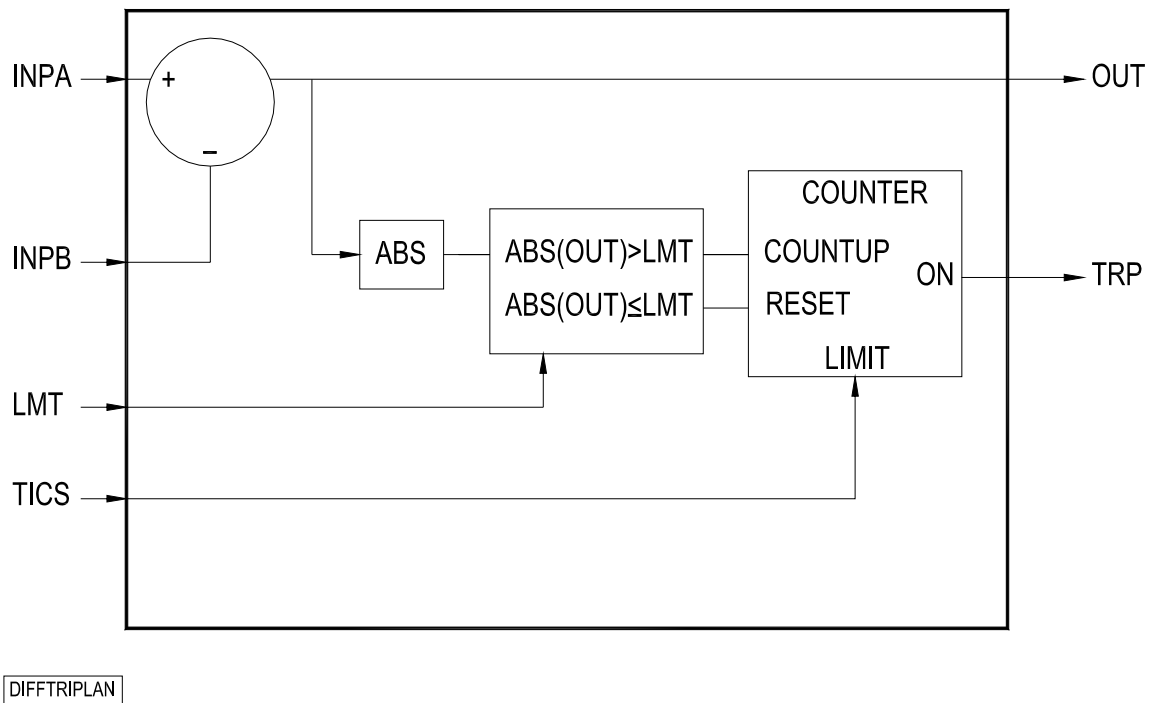


FIGURE 4-28. DIFF TRIP BLOCK

### 1. Inputs

INPA: Analog  
 INPB: Analog  
 TICS: Analog  
 LMT: Analog

### 2. Outputs

OUT: Analog  
 TRP: Bit

### 3. Implementation

OUT is equal to INPA - INPB.

If the absolute value of OUT is greater than LMT, then the internal timer will start to count up each time the block is executed.

When it counts up to the TICS input amount, the TRP output will go high. It will stay high as long as the absolute value of OUT is greater than LMT.

As soon as the limit condition goes false, the timer is reset to zero and the TRP output goes low.

**NOTE:** The amount of time associated with a block execution can vary depending on the application. Look up the TICS input label in Appendix C of the manual for the timing.



## 4.29 DIGITAL IN

The Digital Input block enables the eight digital inputs (USER 7 through USER 14) from the optional FAX-32 board to be mapped to eight consecutive digital data table board addresses.

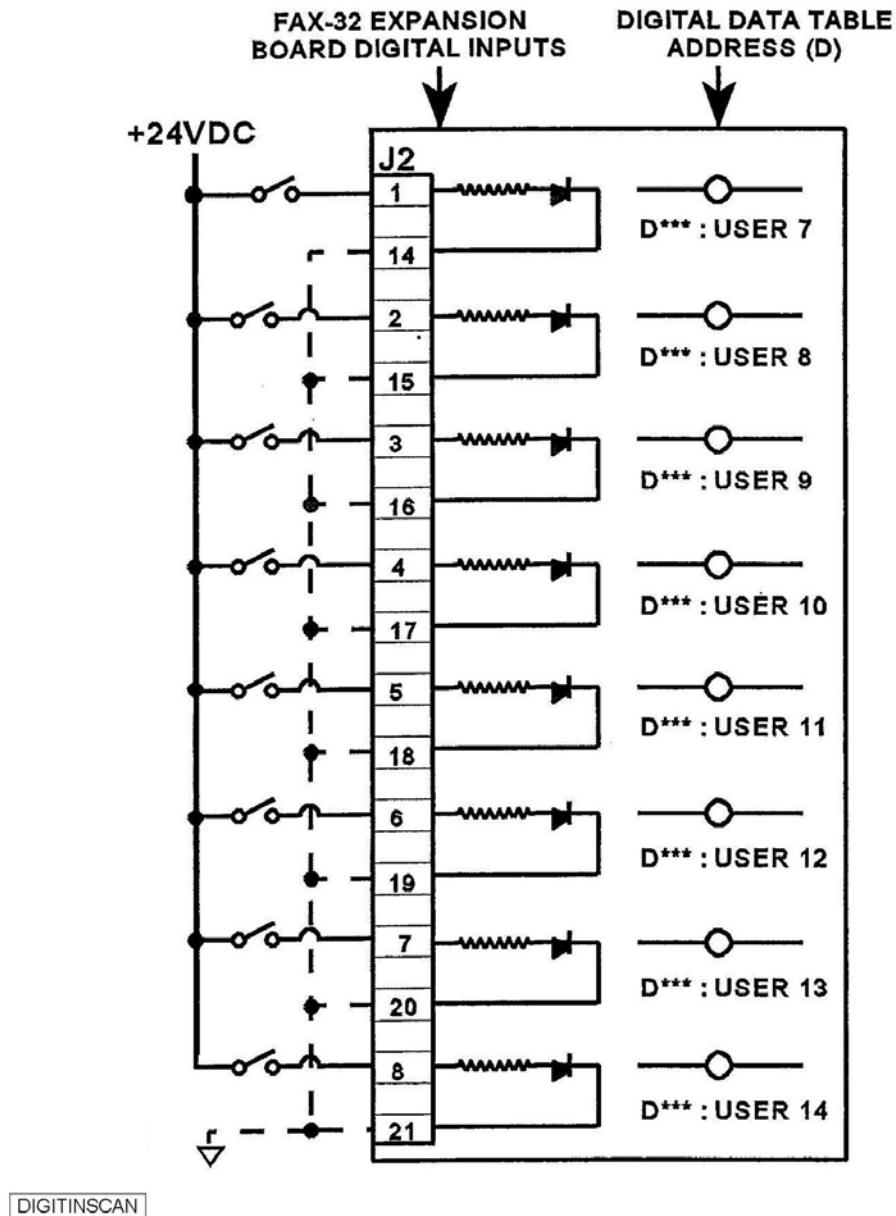


FIGURE 4-29. DIGITAL IN BLOCK

1.     Inputs

Reference FAX-32 digital inputs on J2 of board.

2.     Outputs

START:       BIT

3.     Implementation

The digital input for USER 7 through USER 14 will equal ONE/ON when the input's corresponding FAX-32 J2 terminal is switched to +24 VDC.

The digital input for USER 7 through USER 14 will equal ZERO/OFF when the input's corresponding FAX-32 J2 terminal is switched to 0 VDC.

### 4.30 DIGITAL OR

This block implements a 4 input digital OR.

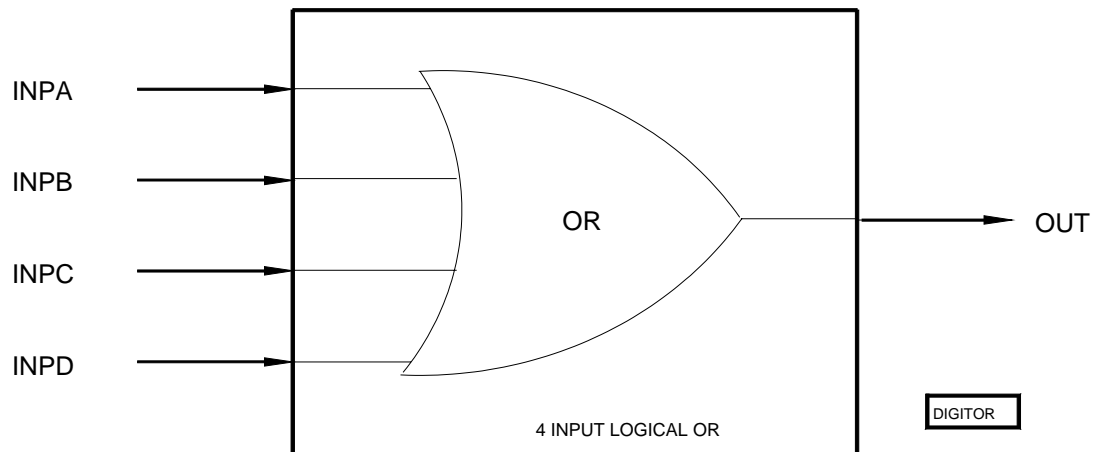


FIGURE 4-30. DIGITAL OR BLOCK

1. Inputs

INPA: Bit  
INPB: Bit  
INPC: Bit  
INPD: Bit

2. Outputs

OUT: Bit

3. Implementation

OUT is set to one if either INPA, INPB, INPC, or INPD is equal to one; otherwise OUT equals zero.

### 4.31 DIVIDE

The Divide block is used to divide two numbers. The block checks for divide by zero to avoid a fault.

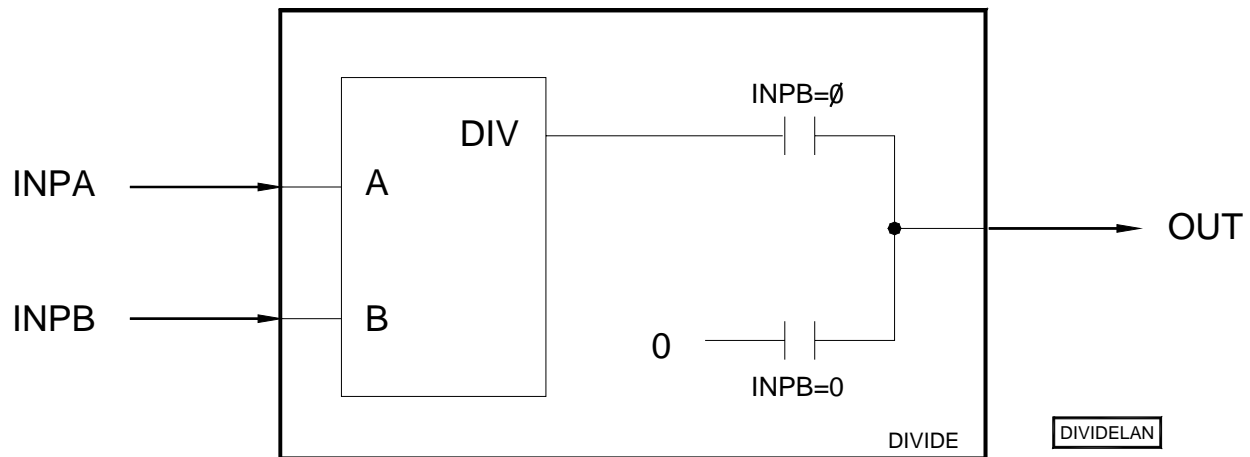


FIGURE 4-31. DIVIDE BLOCK

#### 1. Inputs

INPA: Analog  
INPB: Analog

#### 2. Output

OUT: Analog

#### 3. Implementation

If INPB = 0 then OUT = 0  
else

$$OUT = \frac{INPA}{INPB}$$

### 4.32 DROOP

The Droop block modifies the speed reference to keep the drive armature current within a particular range. This is useful for controlling a nipped roll where it is in contact with another speed controlled section, or anywhere a "SOFT" speed regulator is required.

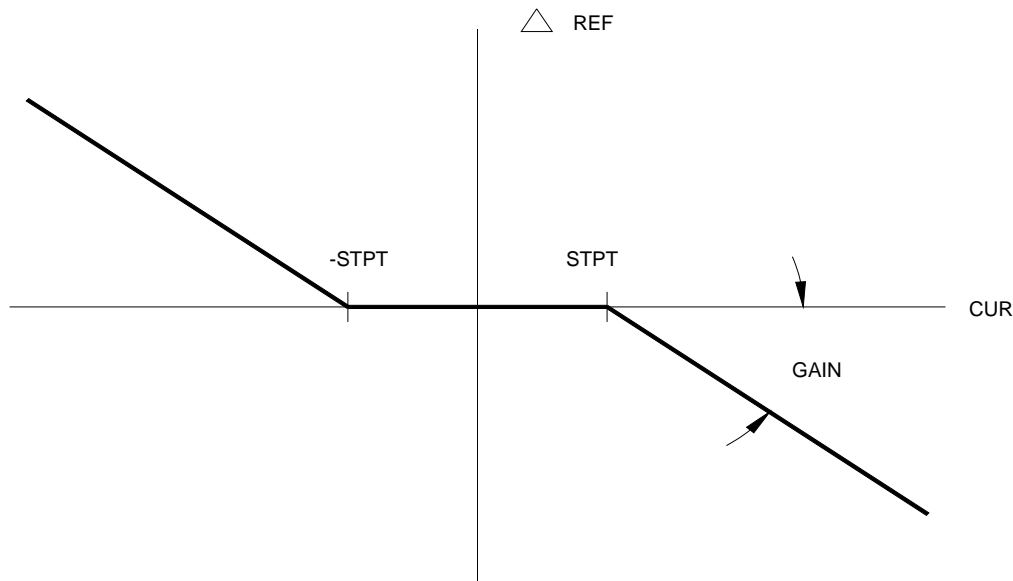


FIGURE 4-32. DROOP BLOCK

#### 1. Inputs

CUR: Analog  
 STPT: Analog  
 GAIN: Analog  
 REF: Analog  
 ENABLE: Bit

#### 2. Outputs

OUT: Analog

#### 3. Implementation

If ENABLE bit low,  $OUT = REF$ .

If ENABLE bit high;

If  $(-STPT) < CUR < STPT$ , then  $OUT = REF$ .

If  $STPT < CUR$ , then  $OUT = (STPT - CUR) \times GAIN + REF$

If  $STPT < -CUR$ , then  $OUT = -(STPT + CUR) \times GAIN + REF$

### 4.33 EIP TOUT

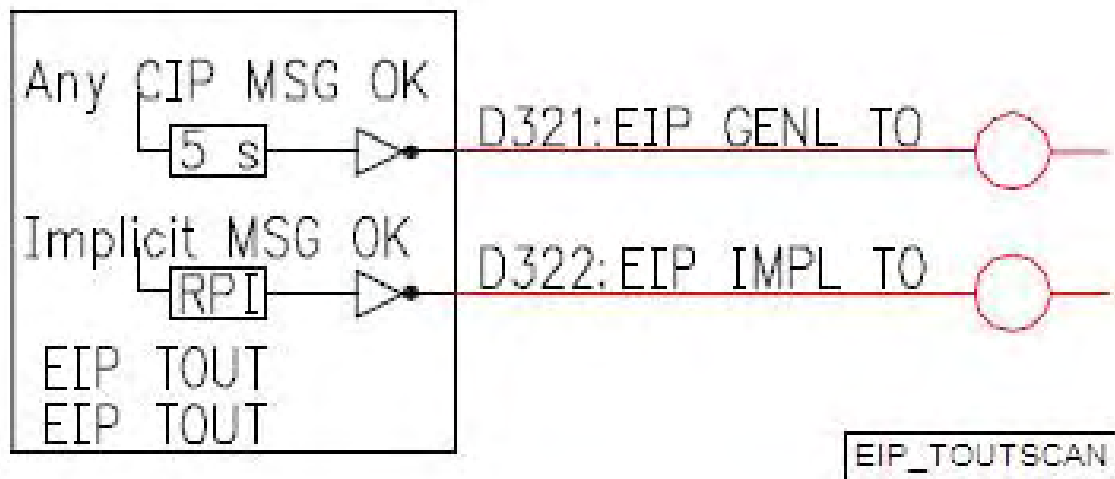


FIGURE 4-33. EIP TOUT BLOCK

1. Inputs

NONE:

2. Outputs

EIP GENL TO	Bit
EIP IMPL TO	Bit

3. Implementation

The EIP TOUT block resides in the ESBX module firmware, versions 682767v16 and later. The outputs of this block are written from the ESBX module directly to the drive application software, digital parameters D321:EIP GENL TO and D322:EIP IMPL TO. The functionality of the block outputs is as follows:

**D321:EIP GENL TO** – This bit will remain low (Zero Bit) while there is at least one CSP message transfer occurring to the ESBX board within 5 seconds. This bit will transition from low to high, 5 seconds following the point where all CIP message transfers are terminated. The bit will reset to a logic level low when CIP message transfers resume. Refer to Appendix I for detailed information regarding the ESBX module interface to Allen-Bradley CSP communication protocol.

**D322:EIP IMPL TO** - This bit will remain at a logic low while the Ethernet/IP *Implicit* message connection to the ESBX board is active and messaging is taking place at a period less than or equal to the R.P.I. (requested packet interval) time the implicit

message is scheduled to occur. This bit will transition from low to high, if the implicit communication becomes inactive for a time period greater than the R.P.I. time the implicit message was scheduled to occur. The bit will reset to a logic level low when *Implicit* messaging resumes. Refer to Appendix I for detailed information regarding the ESBX module interface to Allen-Bradley Ethernet/IP communications protocol.

### 4.34 ERROR

This block is used to generate an error signal such as speed error or current error.

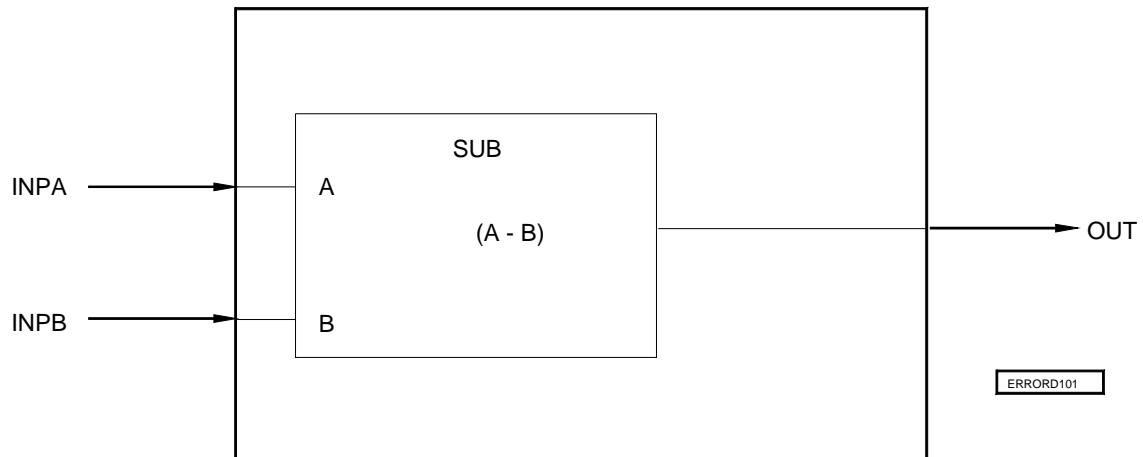


FIGURE 4-34. ERROR BLOCK

1. Inputs

INPA: Analog

INPB: Analog

2. Outputs

OUT: Analog

3. Implementation

$$\text{OUT} = \text{INPA} - \text{INPB}$$



### 4.35 FREQUENCY OUT

The Frequency Out block is used to output a value to the frequency output located on the optional FAX-32 board. For accuracy of the frequency output, the frequency cannot go below 200 Hz. The full range of the frequency output is from 200 to 20,200 Hz. To use the frequency as bidirectional reference, set the offset so 10,100 Hz equals zero; then scale frequency from 20,200 to 200. The INP to the frequency block is user configurable by P\*\*\*:FREQUENCY.

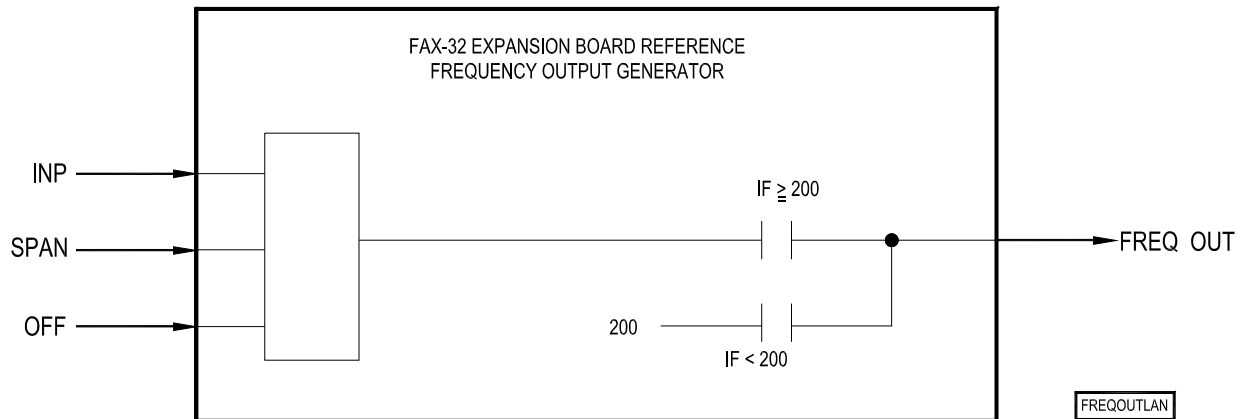


FIGURE 4-35. FREQUENCY OUT BLOCK

#### 1. Inputs

INP:            Analog  
 SPAN:         Analog  
 OFF:           Analog

#### 2. Outputs

Not Applicable

#### 3. Implementation

The output frequency will be:

$$\text{Frequency} = (\text{INP} \times \text{SPAN}) + \text{OFF}$$

Frequency is clamped so as not to go below 200 Hz.

### 4.36 GAIN

The Gain block is used to scale and offset an analog signal.

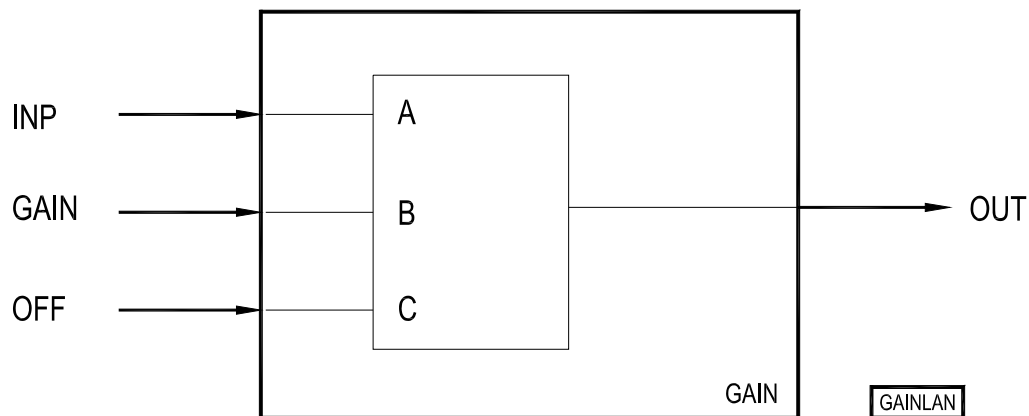


FIGURE 4-36. GAIN BLOCK

#### 1. Inputs

INP: Analog  
GAIN: Analog  
OFF: Analog

#### 2. Outputs

OUT: Analog

#### 3. Implementation

$$\text{OUT} = \text{INP} \times \text{GAIN} + \text{OFF}$$

### 4.37 HI/LOW COMPARATOR

This block sets the appropriate output bits when the input goes out of limits. Corrective action can be taken at this point. Overspeed and AT ZERO SPEED detection are implemented using a HI/LOW Comparator. The user can enable overspeed protection by configuring Y\*\*\*:USR FAULT 2 = OVER SPEED.

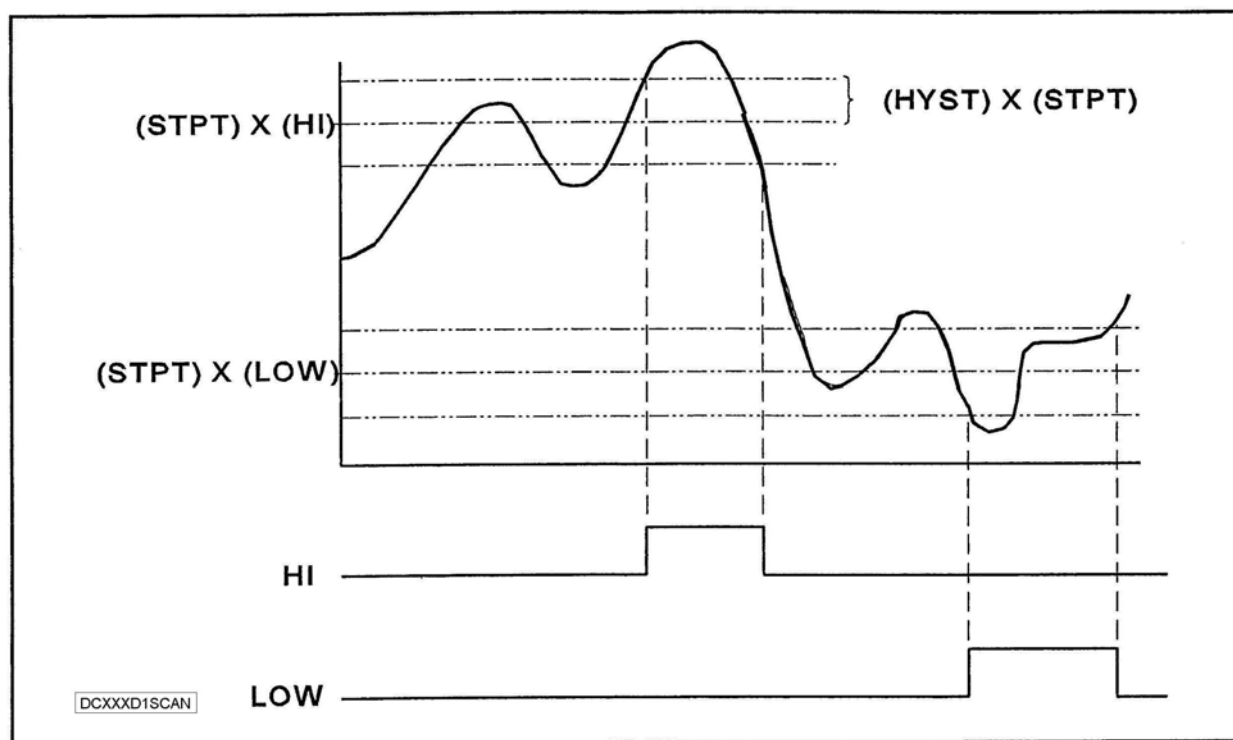


FIGURE 4-37. HI/LO COMPARATOR BLOCK

#### 1. Inputs

HI:	Analog
LOW:	Analog
INP:	Analog
HYS:	Analog
STPT:	Analog

#### 2. Outputs

HI:	Bit
LOW:	Bit

### 3. Implementation

If INP increases so:

$INP - (STPT \times HYS/100) \geq (STPT \times HI/100)$ , HI bit goes high.

If INP decreases so:

$INP + (STPT \times HYS/100) < (STPT \times HI/100)$ , HI bit goes low.

If INP increases so:

$INP - (STPT \times HYS/100) \geq (STPT \times LOW/100)$ , LOW bit goes low.

If INP decreases so:

$INP + (STPT \times HYS/100) < (STPT \times LOW/100)$ , LOW bit goes high.

### 4.38 IIT

#### 1. Inputs

IA	Analog
STPT	Analog
IGN	Analog
FST	Analog
WST	Analog
SQU	Bit
ZER	Bit
IRES	Bit

#### 2. Outputs

VAL	Analog
TRP	Bit
WRN	Bit

#### 3. Implementation

The IIT block is used to determine the current overload for a motor. It can be used when more than one motor is used with the drive.

When IRES is high, the integrator is reset to zero ( $VAL = 0$ ).

When IRES is low, the integrator starts integrating the error.

If ZER is low, then the internal error signal is equal to absolute value of INP minus the STPT input quantity times 0.1.

If ZER is HIGH, the error is equal to  $-(STPT) \times 0.1$ .

This error is fed into the integrator if the SQU input bit is low, giving an IIT function.

If the SQU input is high, then this error is squared (the sign of signal is kept after the squaring) before it goes into the integrator.

The integrator works the same as the PI block with the IGN input as its gain value and VAL as its output.

FST is the upper limit of the integrator output and 0 is the lower limit.

When VAL goes above the WST input, the WRN output bit will go high.

When VAL goes above the FST input, the TRP output bit will go high.

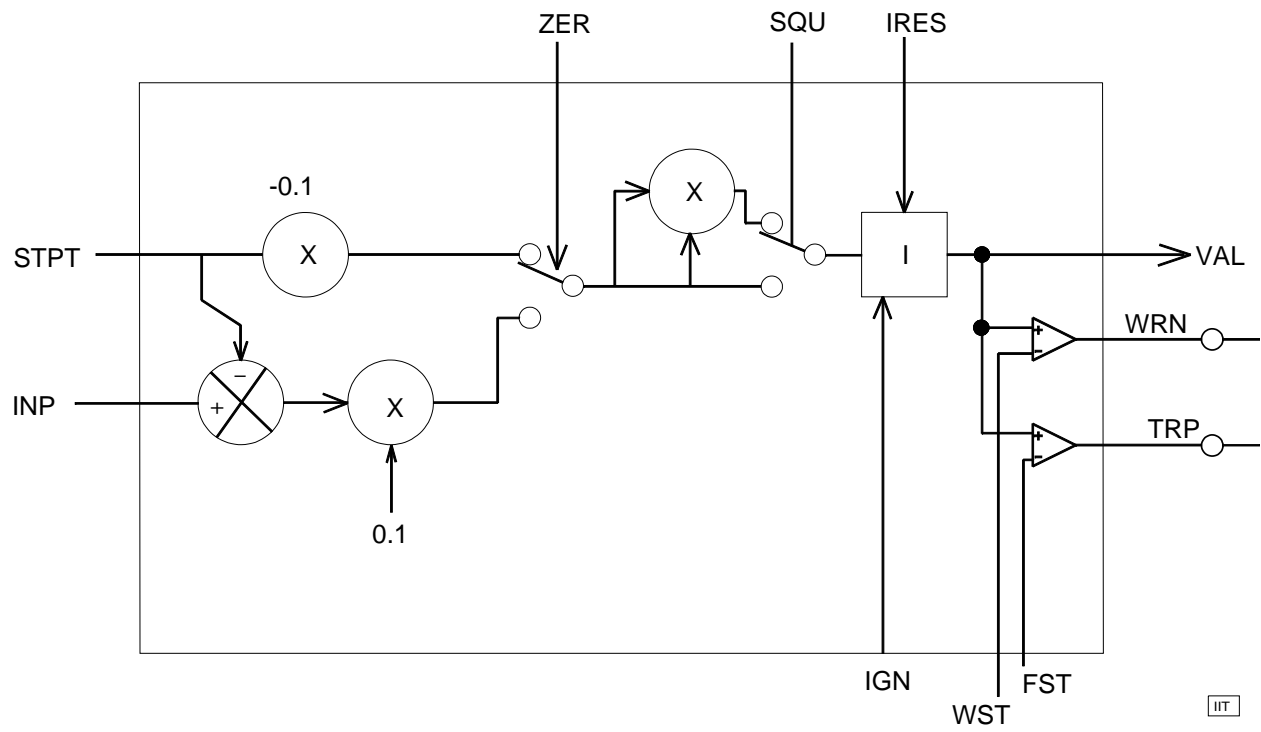


FIGURE 4-38. IIT BLOCK

## 4.39 LATCH

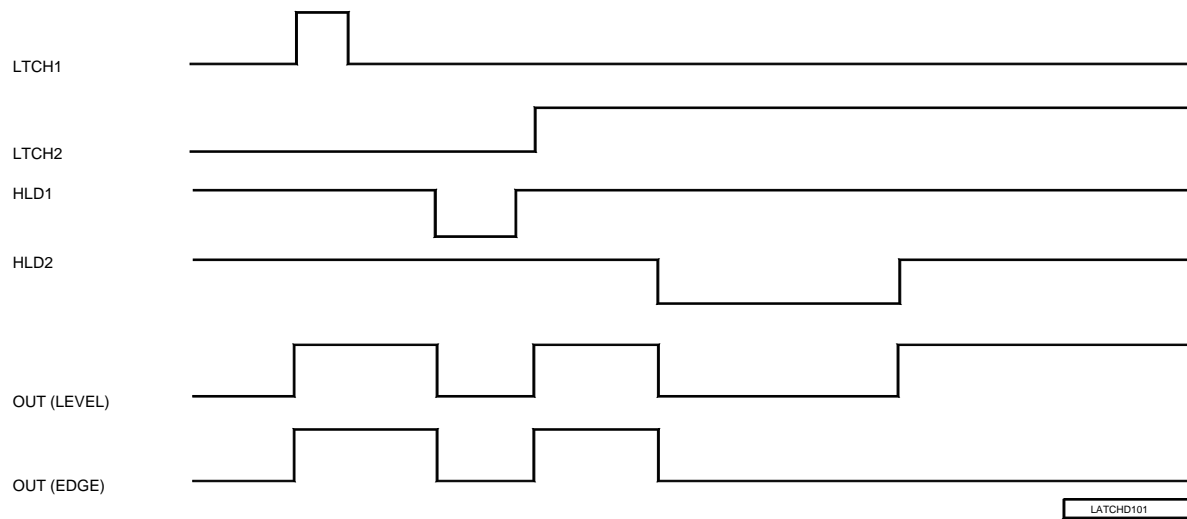


FIGURE 4-39. LATCH BLOCK

### 1. Inputs

LTCH1: Bit  
 LTCH2: Bit  
 HLD1: Bit  
 HLD2: Bit  
 EDGE: Bit

### 2. Outputs

OUT: Bit

### 3. Implementation

If EDGE is low, then:

If either latch (LTCH1 or LTCH2) is high and either hold (HLD1 or HLD2) is high, then OUT goes high and stays high, even if both latches later go low, as long as hold stays high.

When either hold (HLD1 or HLD2) is low, then OUT goes low no matter what the state of the latch bits. The hold inputs have a higher priority than the latch bits. If the hold bits later go high, the condition of OUT will be determined by the condition of the latch bits at that time.

If EDGE is high, then:

If either latch (LTCH1 or LTCH2) transitions to high, the OUT goes high and stays high, even if both latches later go low.

Upon transition of the latch bit high, it does not matter what the state of the hold (HLD1 or HLD2) is in determining the state of the OUT bit, as it does in "If Edge is low."

If OUT is high, when either hold (HLD1 or HLD2) transitions to low, the OUT will go low. It is important to note that the hold must be a transition, not just the current state.



#### 4.40 LEAD/LAG

LEAD COMPENSATION is added to a control loop to improve rise time and the damping. The disadvantage of LEAD COMPENSATION is that it adds instability to the system by increasing high frequency closed loop gain.

LAG/LEAD is added to a control loop to improve overshoot and relative stability. The disadvantage of LAG COMPENSATION is that it results in a lower rise time.

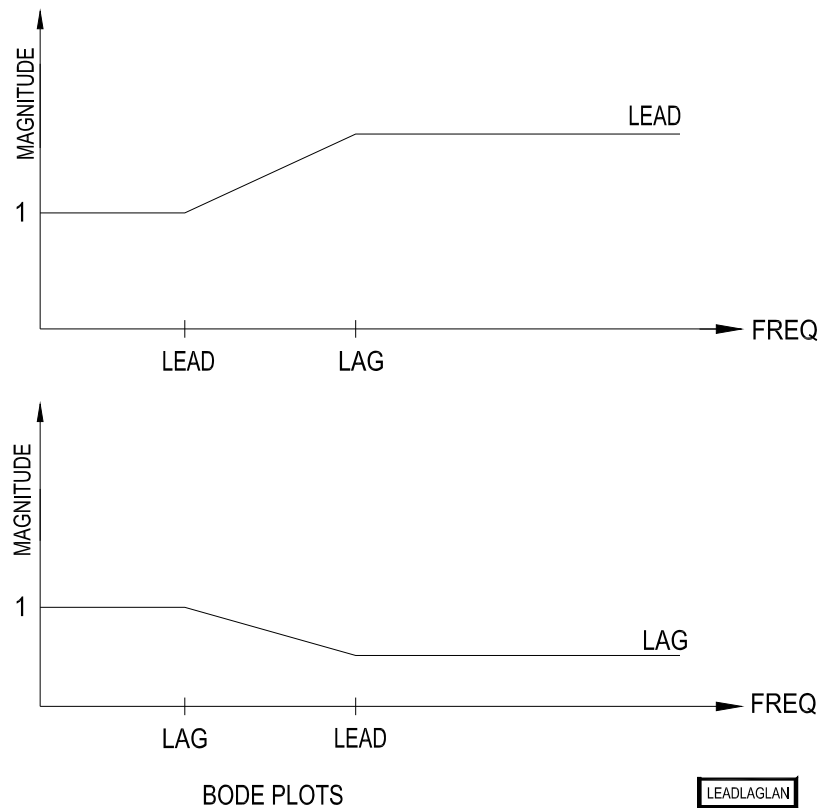


FIGURE 4-40. LEAD LAG BLOCK

##### 1. Inputs

INP: Analog  
 LEAD: Analog  
 LAG: Analog

##### 2. Outputs

OUT: Analog

### 3. Implementation

The LEAD/LAG block is implemented to simulate the following equation.

$$H(s) = \text{LAG/LEAD} \times (s + \text{LEAD}) / (s + \text{LAG})$$

Setting the LEAD value equal to LAG gives the block a unity gain.

#### 4.41 LEAST WIN

The block is used to select the lowest value of the inputs for a setpoint reference.

1. Inputs

INPA:        Analog  
INPB:        Analog  
INPC:        Analog

2. Outputs

OUT:         Analog

3. Implementation

OUT will equal the lowest input value.

e.g.

If        INPA = 40  
          INPB = -20  
          INPC = -30  
  
then     OUT = -30

## 4.42 LOWPASS FILTER

Use to filter out high frequency noise from analog signals, such as tension feedback.

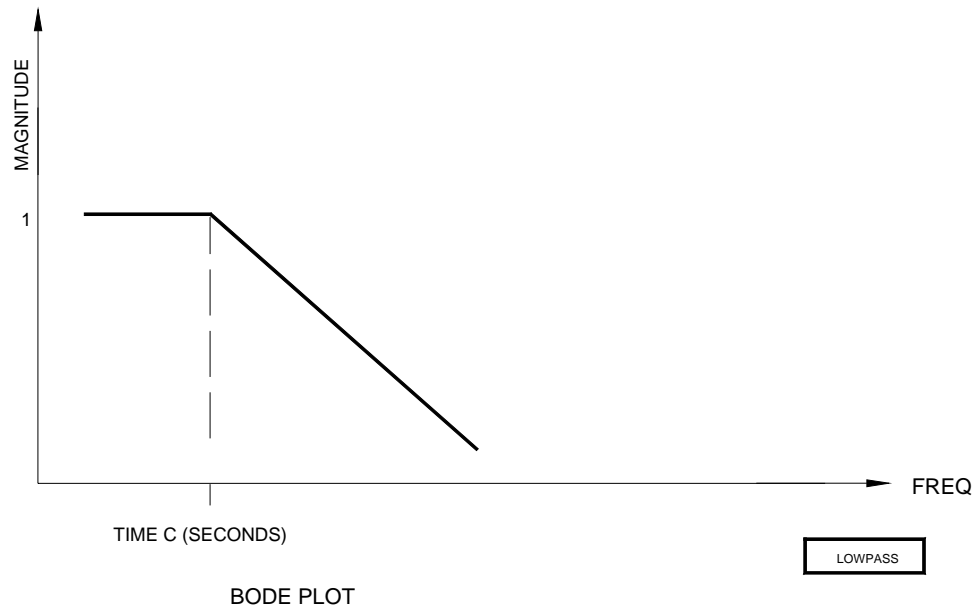


FIGURE 4-42. LOWPASS FILTER BLOCK

### 1. Inputs

INP: Analog  
TC: Analog

### 2. Outputs

OUT: Analog

### 3. Implementation

The lowpass filter takes the INP, filters it for high frequency, then outputs it to OUT. The time constant in seconds for the filter is determined by TC. Limits of the time constant are from 0.00277 to 2.5 seconds.

#### 4.43 MOST WIN

The block is used to select the highest value of the inputs for a setpoint reference.

1. Inputs

INPA: Analog

INPB: Analog

INPC: Analog

2. Outputs

OUT: Analog

3. Implementation

OUT will equal the highest input value.

e.g.

If INPA = 40

INPB = -20

INPC = -30

Then OUT = 40

#### 4.44 MOV8

This block is used to move eight variables to another location, when enabled.

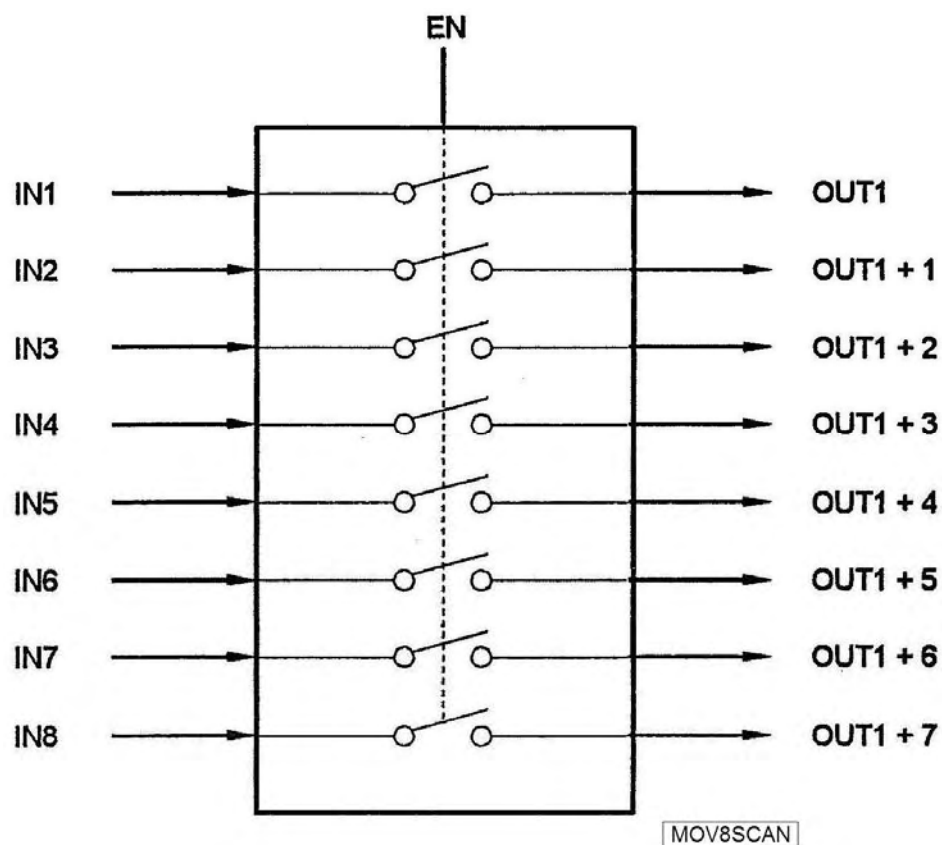


FIGURE 4-44. MOV8 BLOCK

##### 1. Inputs

IN1: Analog  
IN2: Analog  
IN3: Analog  
IN4: Analog  
IN5: Analog  
IN6: Analog  
IN7: Analog  
IN8: Analog

EN: Bit

2. Outputs

OUT1:        Analog

3. Implementation

If EN is low, the output does not change.

When EN is high,

OUT1 =        IN1

Next location =    IN2

Next location =    IN3

Next location =    IN4

Next location =    IN5

Next location =    IN6

Next location =    IN7

Next location =    IN8

#### 4.45 MULTIPLY

This block is used to multiply two analog signals. For example, draw input  $\times$  speed reference signal.

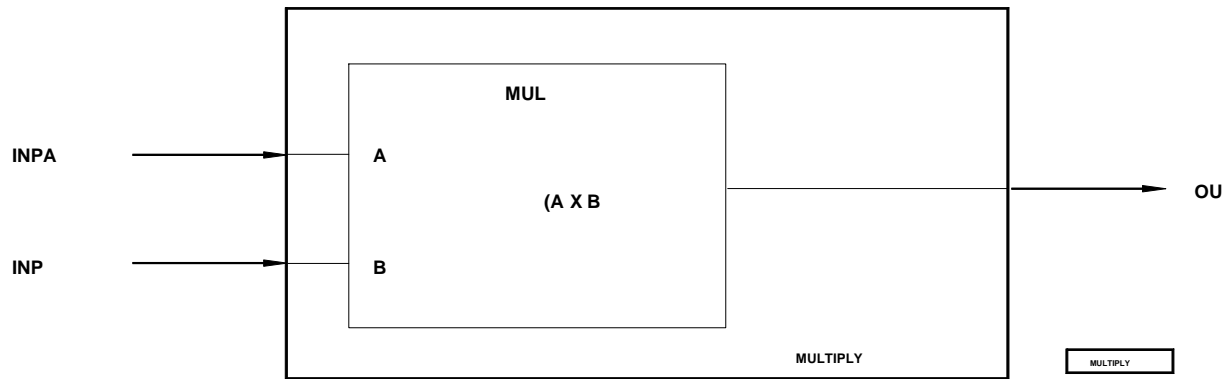


FIGURE 4-45. MULTIPLY BLOCK

1. Inputs

INPA: Analog  
INPB: Analog

2. Outputs

OUT: Analog

3. Implementation

$$\text{OUT} = \text{INPA} \times \text{INPB}$$



## 4.46 NOTCH FILTER

The Notch Filter block is a band reject filter designed to damp out machine resonance. In many cases this resonance is speed independent and occurs at approximately 5-7 Hz.

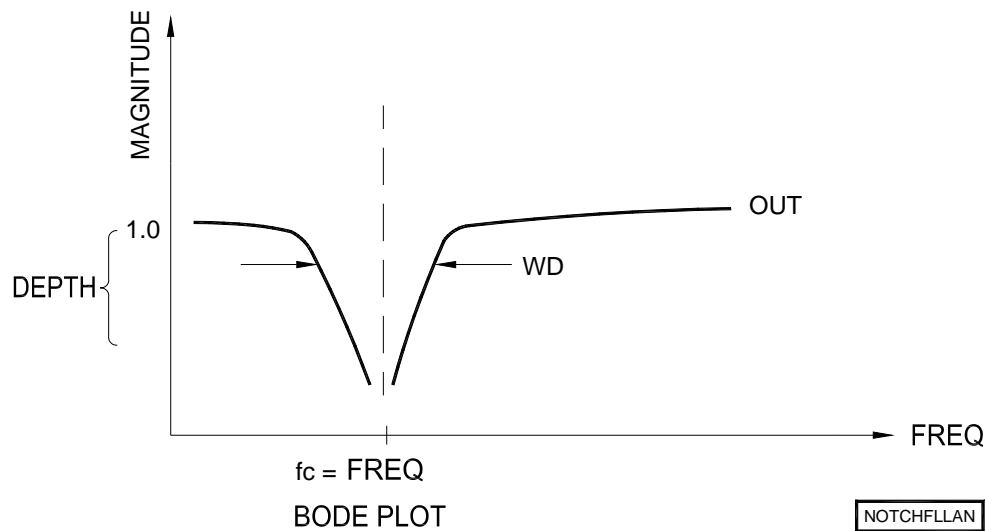


FIGURE 4-46. NOTCH FILTER BLOCK

### 1. Inputs

INP: Analog  
 WD: Analog  
 DEPTH: Analog  
 FREQ: Analog

### 2. Outputs

OUT: Analog

### 3. Implementation

The DEPTH parameter sets the depth of the notch. It can range from 0 to 100. Entering a number less than 2 will yield a notch depth of 0. A depth of 3 will reduce the gain by 1/3 (33%) at frequency point.

The FREQ parameter is used to set the center frequency of the notch. The usable range is from 2 to 15 Hz.

The WD parameter sets the width of the notch and is a unitless quantity ranging from 0.1 to 5.0, where 0.1 is the narrowest and 5.0 is the widest.

For example,  $WD = 2$  will reach approximately 90% of the input at 2 Hz from the frequency point.

#### 4.47 OFF TIMER

The block is used to delay actions after the input bit goes low.

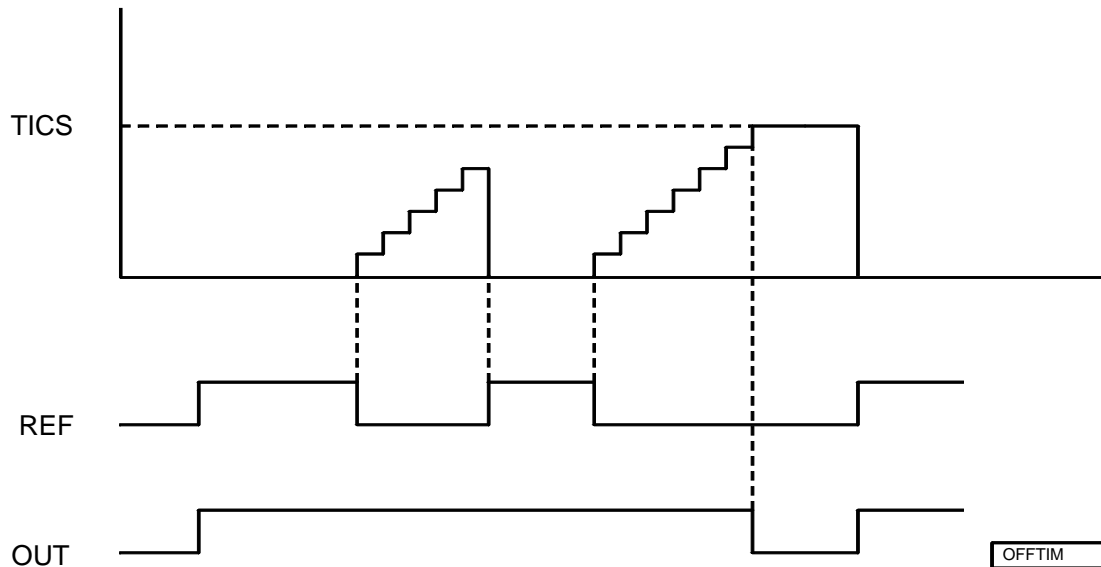


FIGURE 4-47. OFF TIMER BLOCK

1. Inputs

TICS: Analog  
REF: Bit

2. Outputs

OUT: Bit

3. Implementation

If REF is high, then OUT is high.

When REF goes low, the block waits for TICS amount of block executions before OUT goes low. If during the waiting REF goes back high, the counter is reset.

NOTE: The amount of time associated with a block execution can vary depending on the application. Look up the TICS input label in Appendix C of the manual for the timing.

#### 4.48 ON TIMER

1. Inputs

TICS: Analog

REF: Bit

2. Outputs

OUT: Bit

3. Implementation

If REF is low, then OUT is low.

When REF goes high, the block waits for TICS amount of block executions before OUT goes high. If during the waiting REF goes back low, the counter is reset.

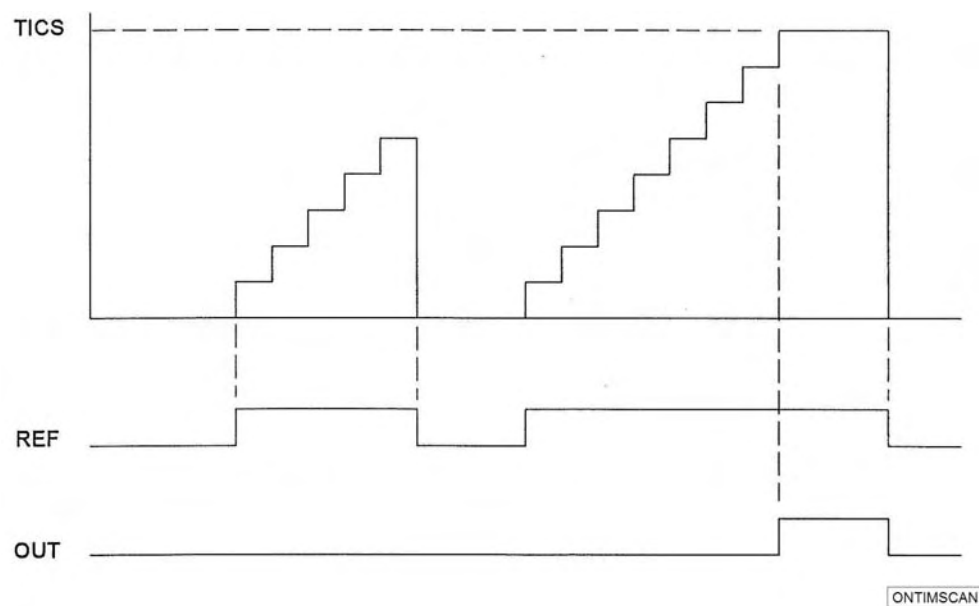


FIGURE 4-48. ON TIMER BLOCK

#### 4.49 ONE SHOT

The block is used to initiate an action only once.

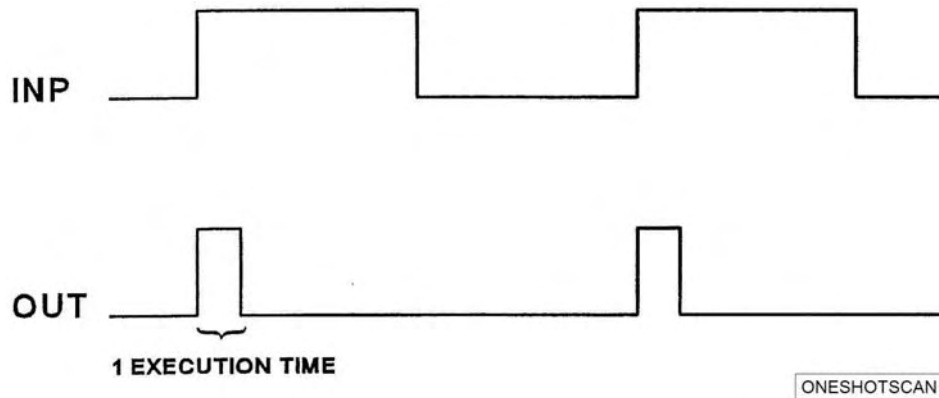


FIGURE 4-49. ONE SHOT BLOCK

1. Inputs

INP: Bit

2. Outputs

OUT: Bit

3. Implementation

If INP is low, then OUT is low.

When INP goes high, OUT will go high for only one execution time.

NOTE: The amount of time associated with a block execution can vary depending on the application. Look up the input or output label in Appendix C of the manual for the timing.

## 4.50 PEAK DETECT

### 1. Inputs

INP	Analog
HLD	Bit
RES	Bit
POS	Bit

### 2. Outputs

OUT	Analog
-----	--------

### 3. Implementation

As long as the RES and HLD bits are low

OUT = the greater of Old OUT or INP (Greatest wins) if POS = 1

OUT = the least of Old OUT or INP (Greatest wins) if POS = 0

If the HLD bit is high, then OUT is held and INP is ignored.

If RES bit is high, OUT = 0.

RES and HLD are both level triggered bits.

RES has higher priority than HLD.

On powerup OUT = 0.

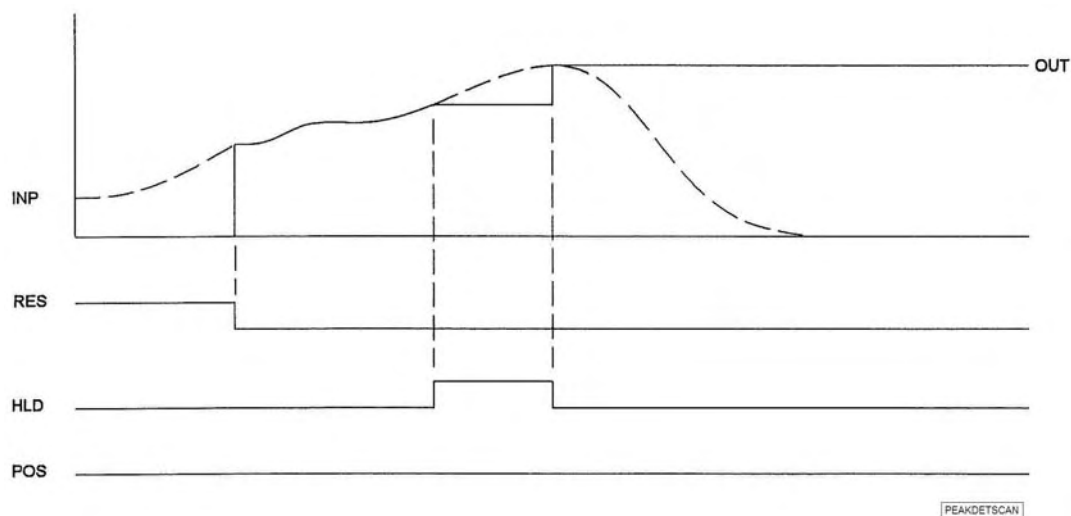


FIGURE 4-50. PEAK DETECT BLOCK

#### 4.51 PERCENT DIFFERENCE

The Percent Difference block indicates that the percent difference between the reference and feedback is greater than the setpoint. It can be used to detect a web loss condition on a center driven winder application.

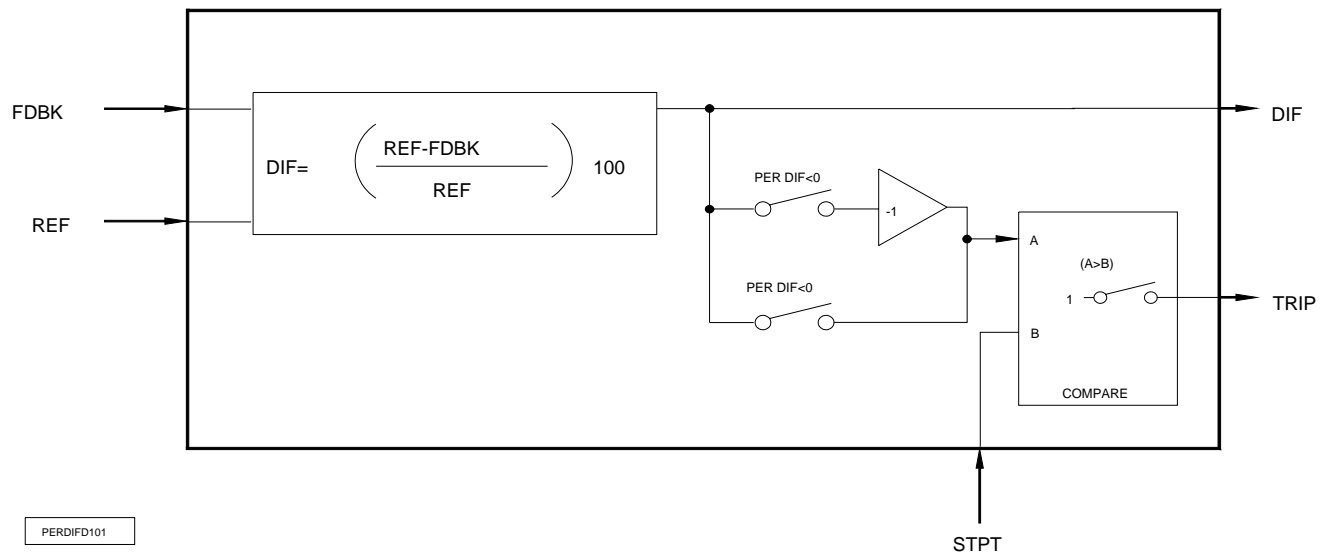


FIGURE 4-51. PERCENT DIFFERENCE BLOCK

##### 1. Inputs

REF: Analog  
FDBK: Analog  
STPT: Analog

##### 2. Outputs

DIF: Analog  
TRIP: Bit

##### 3. Implementation

$$DIF = (1 - FDBK/REF) \times 100$$

TRIP = 1, when the ABSOLUTE | DIF | > STPT, else TRIP = 0

If REF = 0, then DIF = 0

#### 4.52 PERCENT MULTIPLY (Per Mult)

The Percent Multiply block converts percentages entered using the keypad into actual values to be used in other blocks. For example, convert percent current limit into actual current limit.

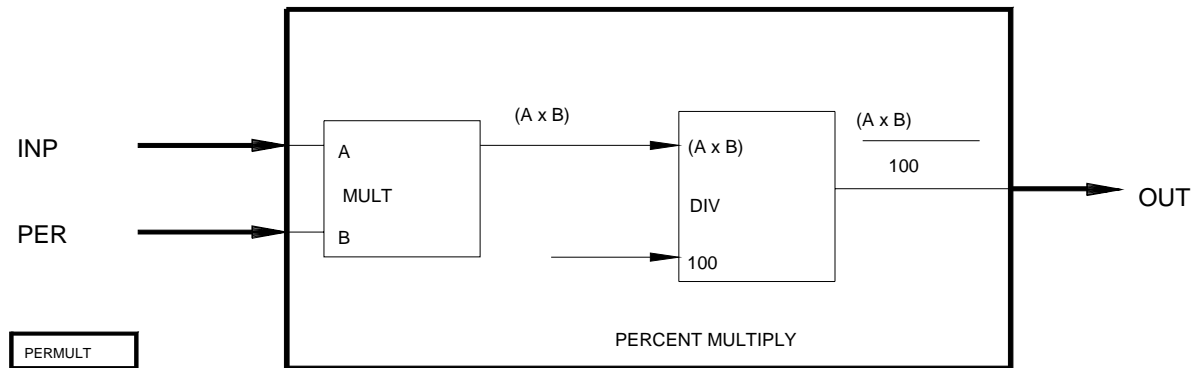


FIGURE 4-52. PERCENT MULTIPLY BLOCK

##### 1. Inputs

PER: Analog  
INP: Analog

##### 2. Outputs

OUT: Analog

##### 3. Implementation

$$OUT = \frac{PER \times INP}{100}$$



### 4.53 PROPORTIONAL AND INTEGRAL CONTROL (PI)

The PI block performs a proportional and integral gain function on an error signal. It has inputs for maximum and minimum limits which prevent the loop from overcompensating.

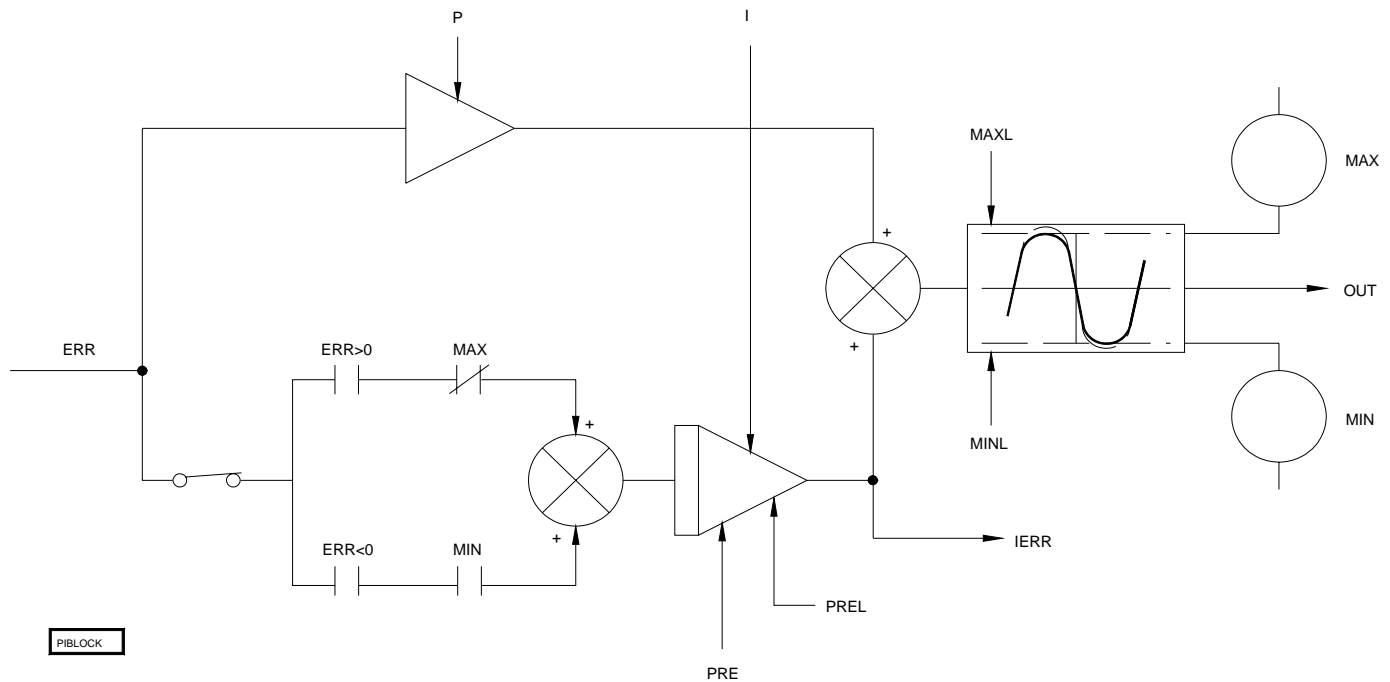


FIGURE 4-53. PI BLOCK

1.	<u>Inputs</u>	<u>Data Type</u>	<u>Description</u>
	ERR:	Analog	Input Signal
	P:	Analog	Proportional Gain Value
	I:	Analog	Integral Gain Value
	MAXL:	Analog	Output High Limit Value
	MINL:	Analog	Output Low Limit Value
	PREL:	Analog	Integrator Preload Value
	HOLD:	Bit	Integrator Hold Enable
	PRE:	Bit	Integrator Preload Enable

2.	<u>Outputs</u>	<u>Data Type</u>	<u>Description</u>
	OUT:	Analog	Output Signal
	IERR:	Analog	Integral Error Value
	MAX:	Bit	Indication Output is Clamped at High Value
	MIN:	Bit	Indication Output is Clamped at Low Value

### 3. Implementation

If HOLD = LOW and PRE = LOW, then:

OUT = Proportional + Integral error values of block

where:

Proportional ERROR (PERR) =  $ERR \times P$

Integral Error (IERR) =

$$\text{Old Integral Error Value} + \frac{ERR}{I \left( \frac{\text{Sample Time}}{1 \text{ Second}} \right)}$$

I is entered in seconds. If I is entered at less than 0.001 seconds, then I is set to zero. The sample time is used to convert to the block execution rate where typically:

Armature Current Loop	= 2.77 msec
Speed Loop	= 8 msec
Tension Loop	= 16 msec

If OUT > MAXL: The following sequence of events will occur:

The MAX bit = 1 (HIGH). The Proportional Error is set so OUT will not exceed MAXL. If the Proportional Error = 0, the Integral Error will start to increase to keep OUT below the MAXL limit.

If OUT < MINL: The following sequence of events will occur:

The MIN bit = 1 (HIGH). The Proportional error component is set so OUT will not exceed MINL. If the Proportional Error = 0, the Integral Error component will start to increase to keep OUT above the MINL limit.

If HOLD = HIGH and PRE = LOW, then:

The Integral Error component is held at its present value until the HOLD input goes low. The integrator hold input is used to hold the output value during major process disturbances.

If PRE = HIGH, then:

The Integral Error component is set to the PREL value and the Proportional Error component is set to zero so that:

$$\text{OUT} = \text{IERR} = \text{PREL}$$

The IERR output is equal to the integrator component and can be used for diagnostic purposes.

#### 4.54 PROPORTIONAL AND INTEGRAL CONTROL WITH CASCADED HOLD BITS (PI2)

The PI2 block performs a proportional and integral gain function on an error signal. It has inputs for maximum and minimum limits which prevent the loop from overcompensating as well as separate bits to hold the integrator in either the positive or negative direction only.

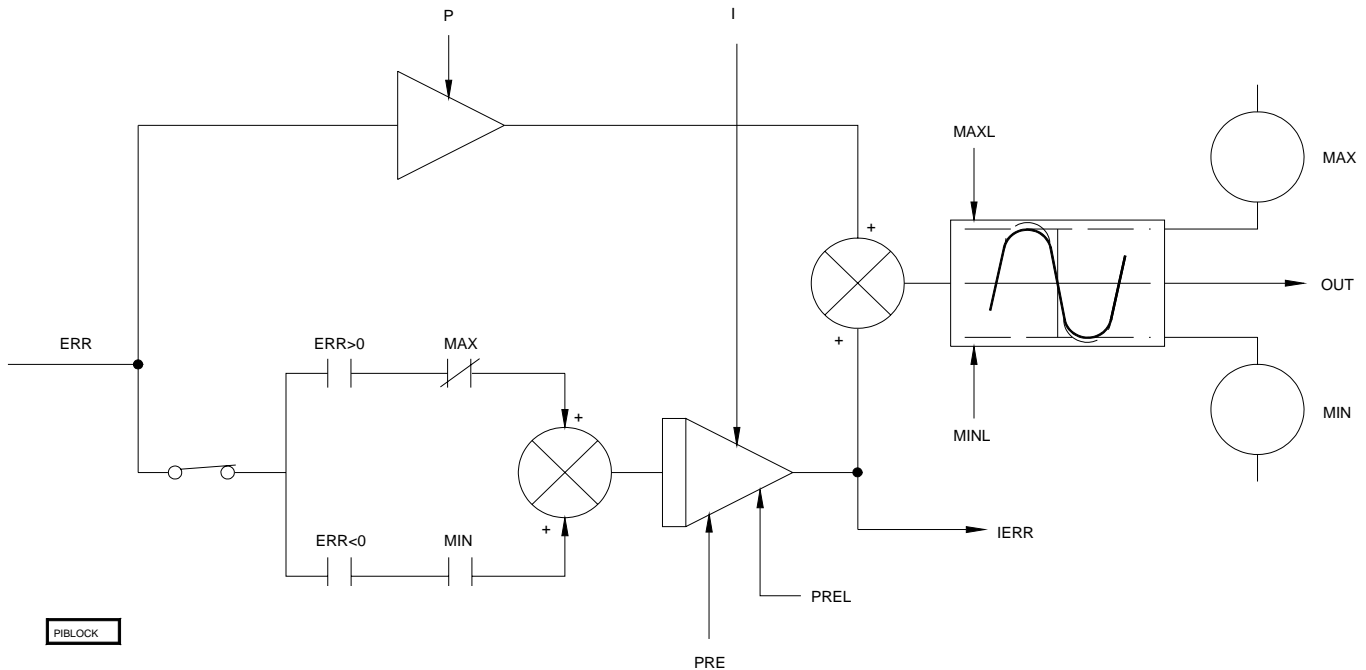


FIGURE 4-54. PI2 BLOCK

1.	<u>Inputs</u>	<u>Data Type</u>	<u>Description</u>
	<b>ERR:</b>	Analog	Input Signal
	<b>P:</b>	Analog	Proportional Gain Value
	<b>I:</b>	Analog	Integral Gain Value
	<b>MAXL:</b>	Analog	Output High Limit Value
	<b>MINL:</b>	Analog	Output Low Limit Value
	<b>PREL:</b>	Analog	Integrator Preload Value
	<b>H-UP:</b>	Bit	Integrator Positive Hold Enable
	<b>H-DN:</b>	Bit	Integrator Negative Hold Enable
	<b>PRE:</b>	Bit	Integrator Preload Enable

2.	<u>Outputs</u>	<u>Data Type</u>	<u>Description</u>
	OUT:	Analog	Output Signal
	IERR:	Analog	Integral Error Value
	MAX:	Bit	Indication Output is Clamped at High Value
	MIN:	Bit	Indication Output is Clamped at Low Value
	CMX:	Bit	Indication Output is Clamped at High Value or is Being Held in the Positive Direction.
	CMN:	Bit	Indication Output is Clamped at Low Value or is Being Held in the Negative Direction.

### 3. Implementation

If H-UP = LOW, H-DN = LOW, and PRE = LOW, then:

$$\text{OUT} = \text{Proportional} + \text{Integral error values of block}$$

where:

$$\text{Proportional ERROR (PERR)} = \text{ERR} \times P$$

$$\text{Integral Error (IERR)} =$$

$$\text{Old Integral Error Value} + \frac{\text{ERR}}{I \left( \frac{\text{Sample Time}}{1 \text{ Second}} \right)}$$

I is entered in seconds. If I is entered at less than 0.001 seconds, then I is set to zero. The sample time is used to convert to the block execution rate where typically:

$$\begin{aligned} \text{Armature Current Loop} &= 2.77 \text{ msec} \\ \text{Speed Loop} &= 8 \text{ msec} \\ \text{Tension Loop} &= 16 \text{ msec} \end{aligned}$$

If OUT > MAXL: The following sequence of events will occur:

The MAX bit = 1 (HIGH). The Proportional Error is set so OUT will not exceed MAXL. If the Proportional Error = 0, the Integral Error will start to increase to keep OUT below the MAXL limit.

If OUT < MINL: The following sequence of events will occur:

The MIN bit = 1 (HIGH). The Proportional error component is set so OUT will not exceed MINL. If the Proportional Error = 0, the Integral Error component will start to increase to keep OUT above the MINL limit.

If  $OUT > MAXL$  or  $H-UP = 1$ : The CMX bit = 1 (HIGH).

If  $OUT < MINL$  or  $H-DN = 1$ : The CMN bit = 1 (HIGH).

If  $H-UP = HIGH$  and  $PRE = LOW$ , then:

The Integral Error component cannot increase in the positive direction until the H-UP input goes low. Positive ERR values are ignored by the integral error component. The integrator hold up input is used to keep the integrator from increasing in the positive direction during major process disturbances. Note that the Proportional Error is not affected by the H-UP input.

If  $H-DN = HIGH$  and  $PRE = LOW$ , then:

The Integral Error component cannot increase in the negative direction until the H-DN input goes low. Negative ERR values are ignored by the integral error component. The integrator hold down input is used to keep the integrator from increasing in the negative direction during major process disturbances. Note that the Proportional Error is not affected by the H-DN input.

If  $PRE = HIGH$ , then:

The Integral Error component is set to the PREL value and the Proportional Error component is set to zero so that:

$$OUT = IERR = PREL$$

The IERR output is equal to the integrator component and can be used for diagnostic purposes.

## 4.55 QUAD LTCH

### 1. Inputs

BIT1: Bit  
 BIT2: Bit  
 BIT3: Bit  
 BIT4: Bit  
 EN: Bit

### 2. Outputs

OUT1 Bit  
 OUT2 Bit  
 OUT3 Bit  
 OUT4 Bit

### 3. Implementation

On a low to high transition of the EN input, the following outputs are sampled.

If BIT1 = 1 then OUT1 = 1 else OUT1 = 0

If BIT2 = 1 then OUT2 = 1 else OUT2 = 0

If BIT3 = 1 then OUT3 = 1 else OUT3 = 0

If BIT4 = 1 then OUT4 = 1 else OUT4 = 0

If EN is low on power-up, then all outputs will equal 0.

If EN is high on power-up, then sample the bits.

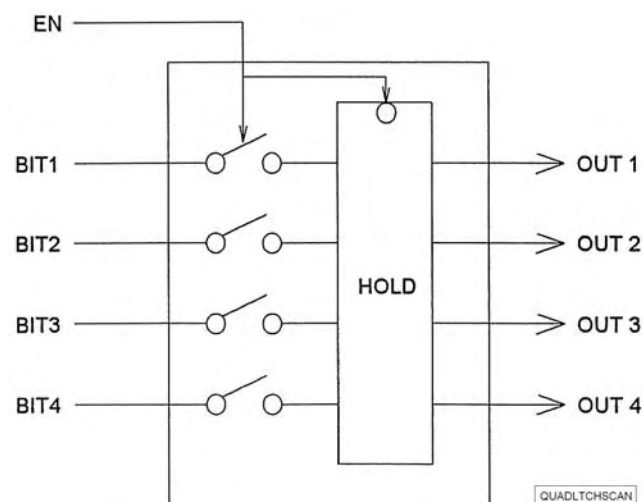


FIGURE 4-55. QUAD LTCH BLOCK

## 4.56 RAMP

The Ramp block provides a variable rate linear ramp with user programmable smoothing. The purpose of this block is to provide a smooth reference from changing setpoint values.

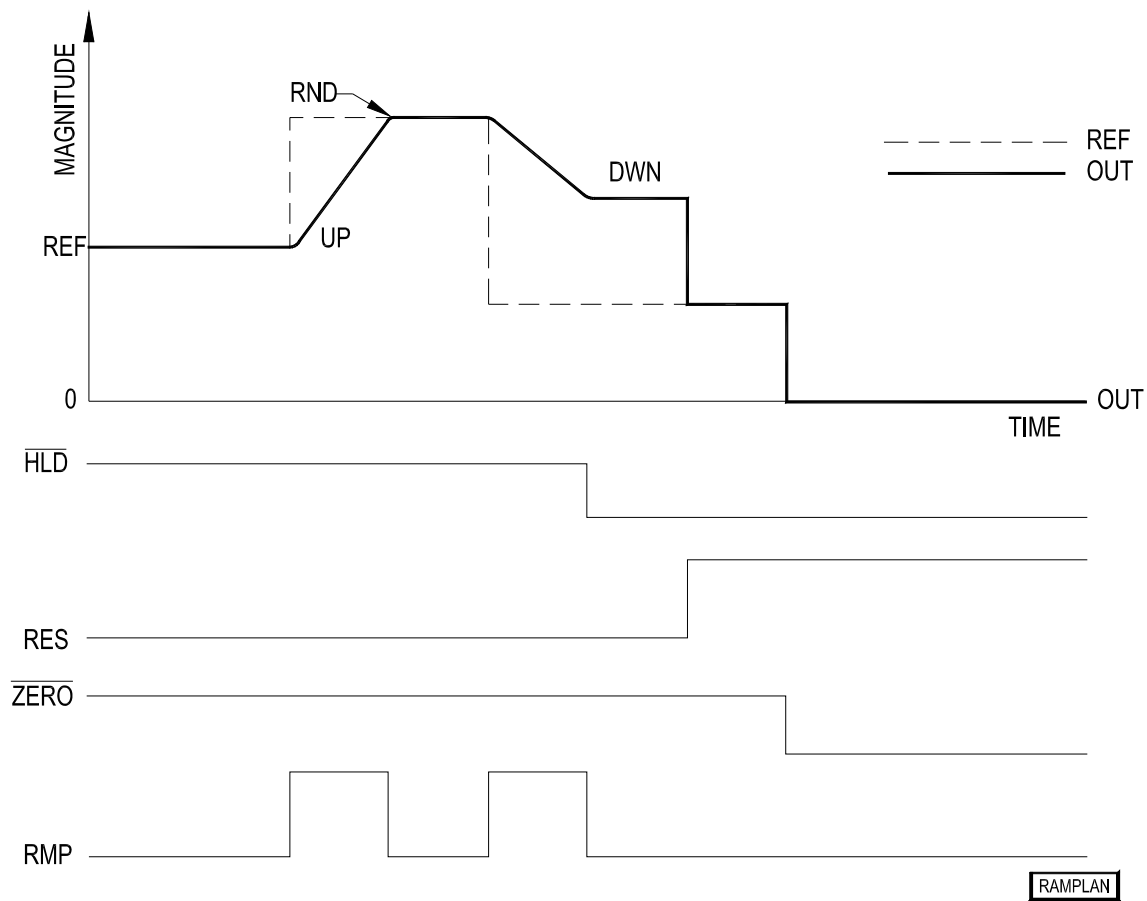


FIGURE 4-56. RAMP BLOCK

### 1. Inputs

REF: Analog  
 UP: Analog  
 DWN: Analog  
 RND: Analog  
 RES: Bit

$\overline{\text{HLD}}$ : Bit

$\overline{\text{ZERO}}$ : Bit



## 2. Outputs

OUT:           Analog  
RMP:           Bit

## 3. Implementation

If  $\overline{\text{ZERO}}$  bit is low,  $\text{OUT} = 0$ . When  $\overline{\text{ZERO}}$  bit goes high, OUT ramps to REF by the UP or DWN ramp rates. (Highest bit priority.)

If the RES bit is high,  $\text{OUT} = \text{REF}$ . (Second in priority.)

If the  $\overline{\text{HLD}}$  bit is low, OUT is held at its present value. The rounding continues to prevent a step response. When  $\overline{\text{HLD}}$  goes high, OUT ramps to REF by the appropriate rate.

The UP/DWN inputs are entered in units/second.

The following holds true while the  $\overline{\text{HLD}}$ ,  $\overline{\text{ZERO}}$  bits are set high and the RES bit is low:

If REF is increasing faster than UP, the RMP bit is set high and OUT ramps at the UP value. If UP is equal to zero, then the OUT ramps with the REF. If REF decreases faster than DWN, the RAMP bit is set high and OUT ramps at the DWN value. If DWN is equal to zero, then the OUT ramps with the REF. If neither of the preceding conditions are true, the RMP bit is set low and OUT equals REF.

The RND input determines the amount of S-ramp to be applied to the OUT. This is implemented as a low pass filter to the linear ramp. The RND value is entered as a time constant in seconds. If  $\text{RND} < .005$ , no rounding will take place.

### **NOTE**

On powerup,  $\text{OUT} = \text{REF}$ .

## 4.57 RATE CHANGE

This block is used to restrict the rate of change of an analog signal to a user programmable maximum rate limit.

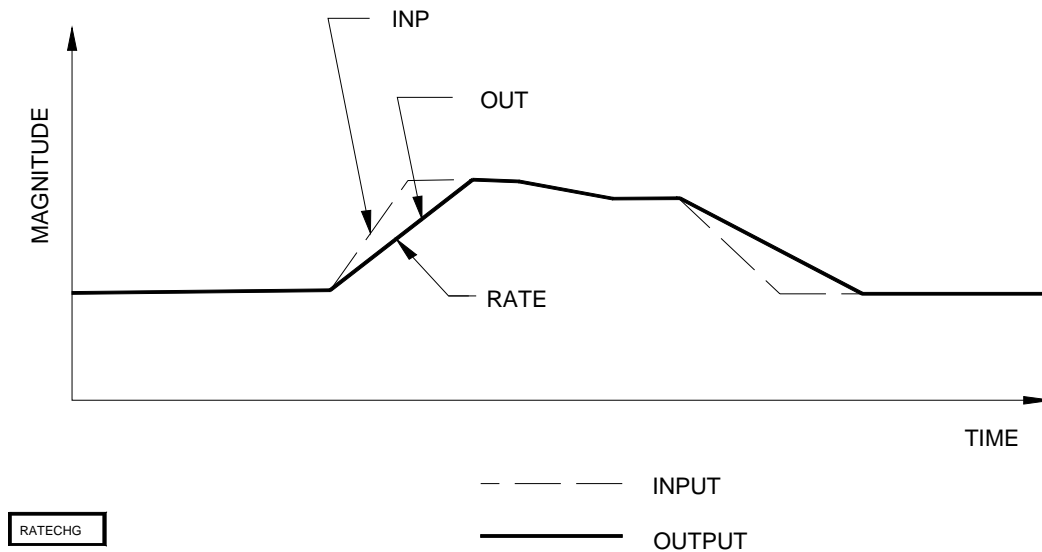


FIGURE 4-57. RATE CHANGE BLOCK

### 1. Inputs

INP:        Analog  
RATE :     Analog

### 2. Outputs

OUT:        Analog

### 3. Implementation

RATE is scaled in units/second.

If INP is changing less than RATE, OUT is equal to INP. If INP is changing faster than RATE, OUT changes at the RATE value.

## 4.58 RATIO

The Ratio Block calculates the diameter of a center driven winder. It can be used for a winder or an unwinder. The initial diameter is a preset input value to obtain the correct diameter starting speed.

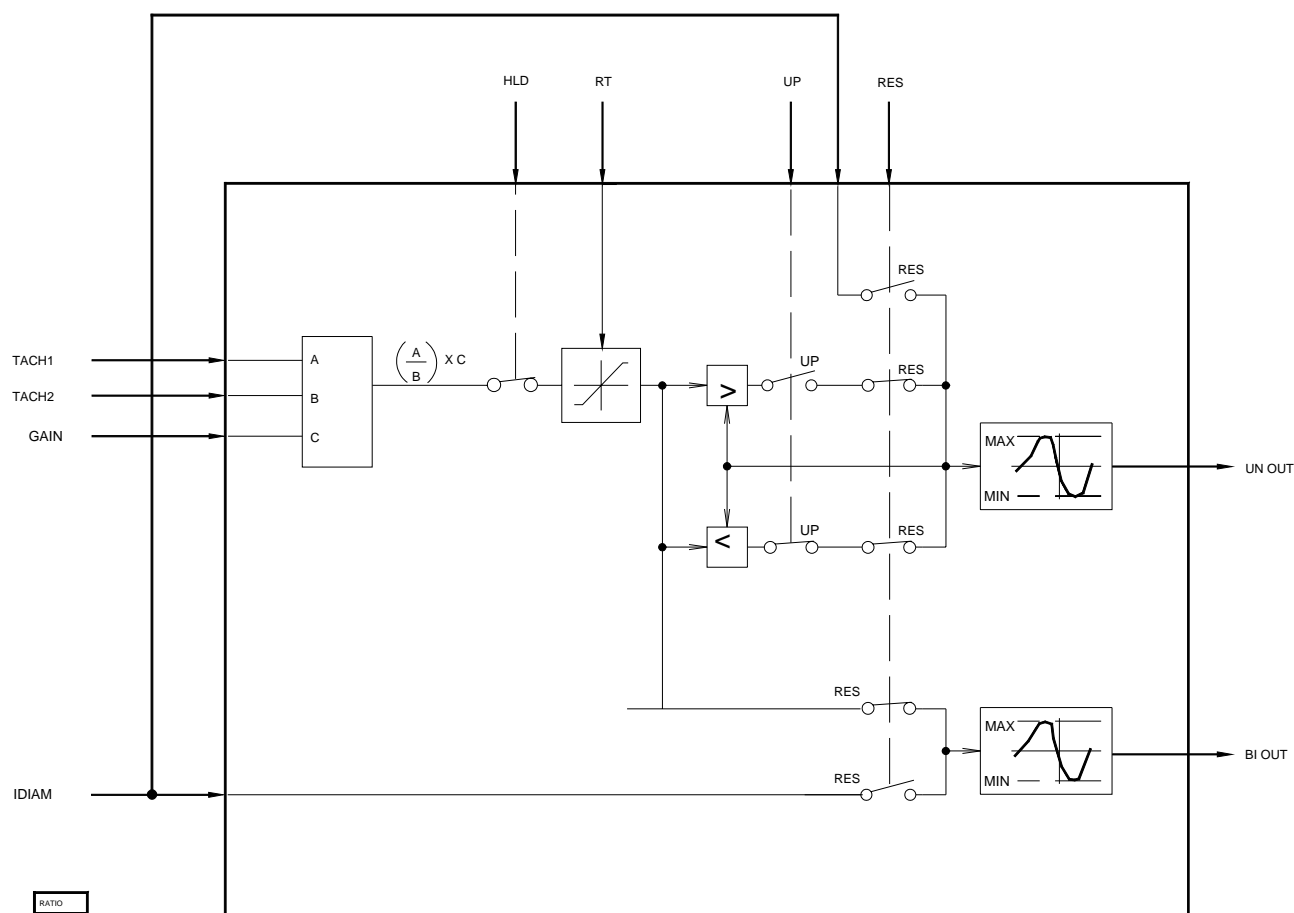


FIGURE 4-58. RATIO BLOCK

### 1. Inputs

IDIAM:	Analog
TACH1:	Analog
TACH2:	Analog
GAIN:	Analog
MAX:	Analog
MIN:	Analog
RT:	Analog
HLD:	Bit

Inputs (Cont.)

UP: Bit  
RES: Bit  
RET: Bit

2. Outputs

BIOUT: Analog  
UNOUT: Analog

3. Implementation

$[(TACH1/TACH2) \times GAIN] = BIOUT$  if it is within MIN and MAX, else BIOUT will equal the limit value. BIOUT is rate limited by the RT value. RT is entered in units/second and should be set at maximum rate of change at core at max speed.

If the HOLD bit goes high, then BIOUT and UNOUT will be held at their current values. Releasing this bit lets the block resume calculations.

If UP bit is high, then UNOUT equals the highest BIOUT since the last reset. If the UP bit is low, then the UNOUT equals the lowest BIOUT since the last reset.

The RES bit is used to reset both BIOUT and UNOUT to the IDIAM value. It stays at this value as long as the RES bit is high. The RES bit has a higher priority than the HOLD bit.

Non-retentive Block

On powerup of the ADDvantage-32,  $UNOUT = IDIAM$   
 $BIOUT = IDIAM$

Retentive Block

On powerup of the ADDvantage-32, BIOUT and UNOUT will be initialized under the following conditions:

If  $RET = 0$ , then  $UNOUT = IDIAM$  and  
 $BIOUT = IDIAM$

If  $RET = 1$ , UNOUT and BIOUT are set to their last value. UNOUT and BIOUT must also be configured to retentive points to be updated automatically on powerup.

## 4.59 RECIPE

### 1. Inputs

RECA:	Analog
RECB:	Analog
RECC:	Analog
ENA:	Bit
ENB:	Bit
ENC:	Bit
EN:	Bit

### 2. Outputs

OUT:	Analog
FLT:	Bit

### 3. Implementation

RECA, RECB, RECC points to the first address of 10 consecutive calibration locations.

OUT points to the first address of 10 consecutive analog locations.

On power up, the OUT locations (10 values) are set to the RECA values.

When the EN bit is high, the block will select which block of 10 values to output based on the ENA, ENB, and ENC bits.

ENA transfers RECA data.

ENB transfers RECB data.

ENC transfers RECC data.

When EN is low, no transitions occur.

ENA has the highest priority and is also used when no enable is present.

ENB is the second highest priority.

On power up, FLT output bit is low.

Whenever EN is enabled, the FLT output is checked. FLT will go high if no bits are selected or if more than one is selected.

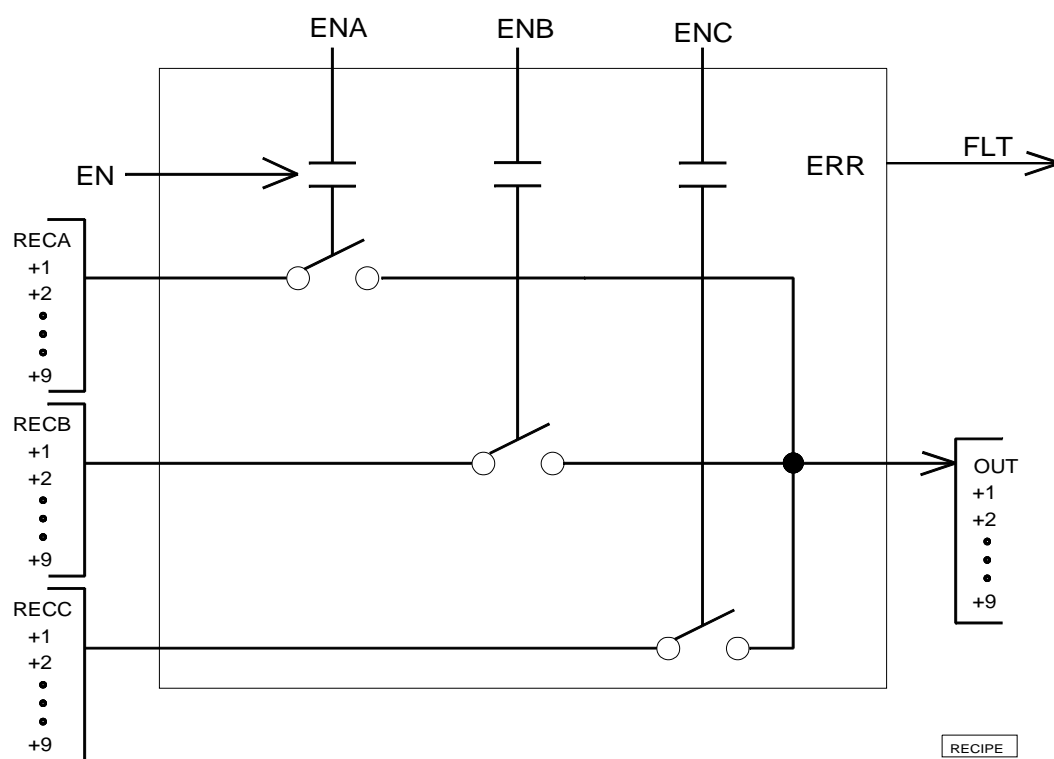


FIGURE 4-59. RECIPE BLOCK

## 4.60 RESOLVER 1

The RESOLVER 1 block is only used in conjunction with the Avtron optional Resolver board. The Resolver board mounts on the first SBX site on the Maxi system board. It provides 16 digital inputs and two digital outputs. This block provides the software interface to the board.

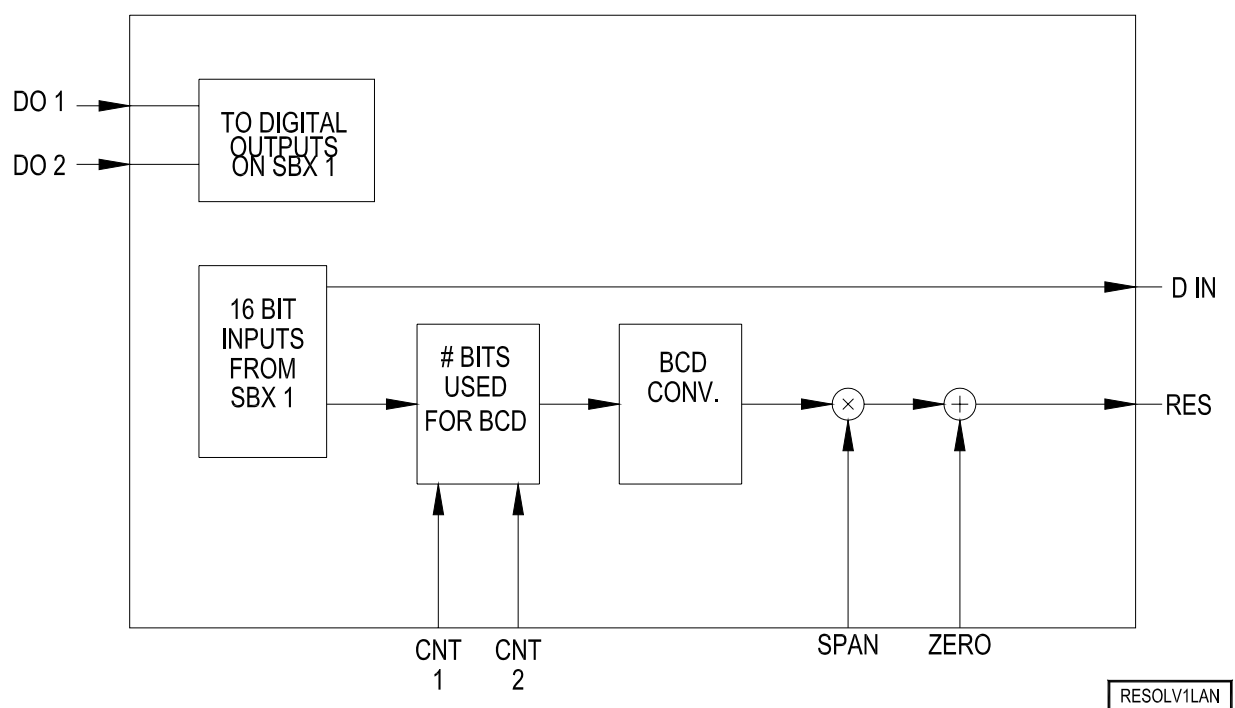


FIGURE 4-60. RESOLVER 1 BLOCK

### 1. Inputs

SPAN: Analog  
 ZERO: Analog  
 DO 1: Digital  
 DO 2: Digital  
 CNT 1: Digital  
 CNT 2: Digital

### 2. Outputs

RES: Analog  
 D IN: Digital

### 3. Implementation

DO 1 and DO 2 bits control the two digital outputs on the resolver board. When they are equal to one, the corresponding output is high.

CNT 1 and CNT 2 decide how many of the input bits are used in a BCD conversion for a resolver as follows:

CNT 1	CNT 2	Number of bits used
0	0	4 bits
1	0	8 bits
0	1	12 bits
1	1	16 bits

The number of bits determined by the above table is then converted to a BCD number and then scaled to the block's output value (RES) as follows:

$$(\text{BCD number} \times \text{SPAN}) + \text{ZERO} = \text{RES}$$

EXAMPLE:

-CNT 1: LOW  
-CNT 2: HIGH

-INPUT BITS	0100	0101	0000
-------------	------	------	------

-BCD VALUE	4	5	0
------------	---	---	---

-SPAN = 2

-OFF = 100

-RES =  $(450 \times 2) + 100 = 1,000$

All 16 input bits are outputted as digital bits in consecutive order starting at D IN location. Name the next 16 locations, but do not connect them to an output of another block or unpredictable results will occur.



## 4.61 RMP2

The RMP2 block provides a variable rate linear ramp with user programmable smoothing. The purpose of this block is to provide a smooth reference from changing setpoint values.

The difference between the RAMP block and RMP2 is the RND input. RAMP uses a low-pass filter for rounding, causing a "J" curve. The RMP2 implements a rate of change limit on the ramp, causing a uniform "S" curve.

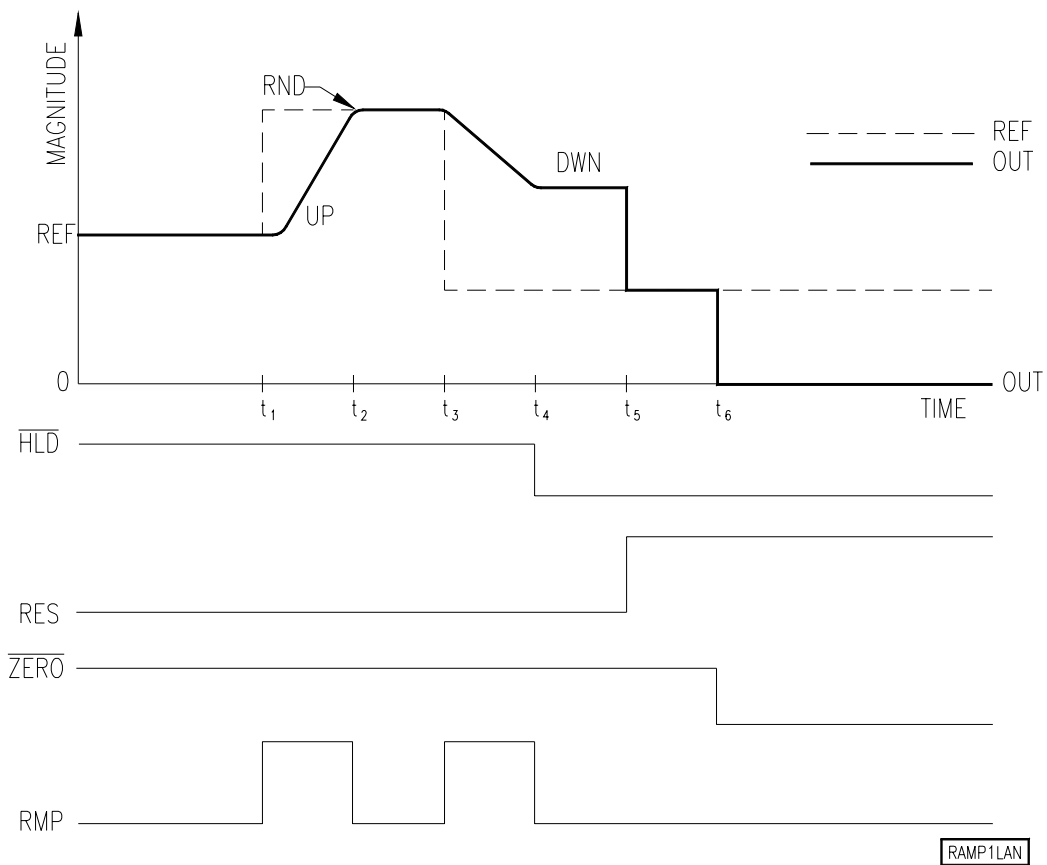


FIGURE 4-61. RMP2 BLOCK

The RMP2 block can be divided internally into three components to aid in the understanding of its operation. These components are a Ramp Change Block, a Rate of Change Limit Block, and Additional Control I/O as can be seen in Figure 4-61A.

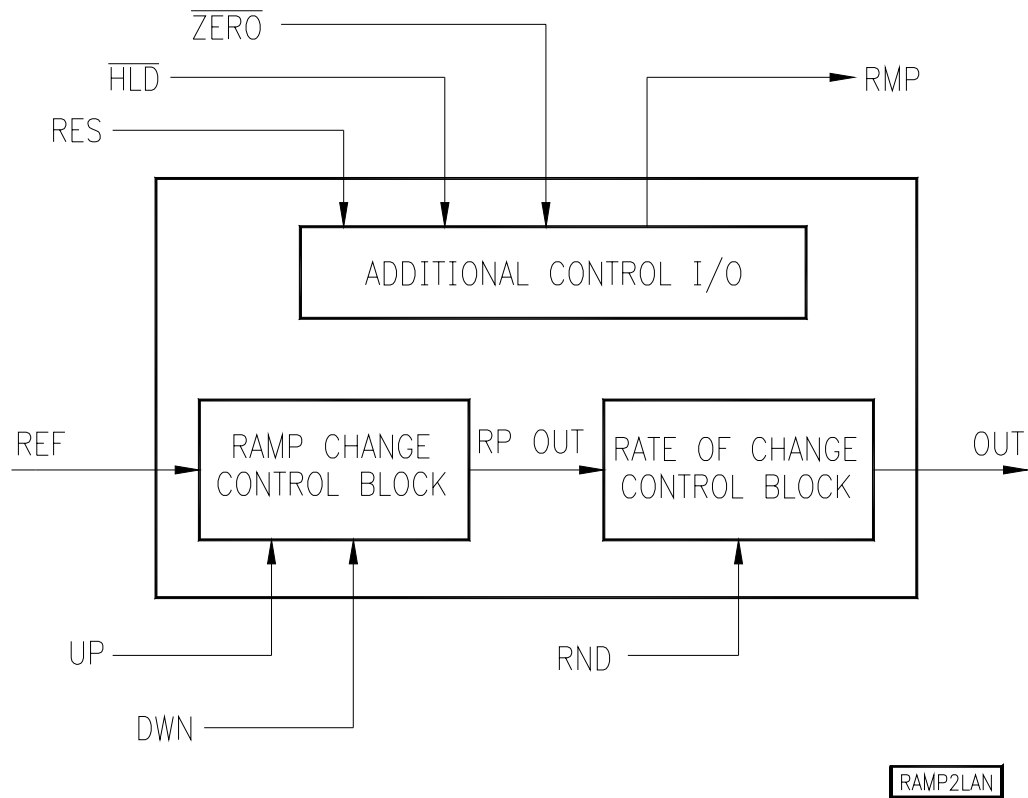


FIGURE 4-61A

### RAMP CHANGE BLOCK

#### 1. Inputs

UP:            Analog  
 DWN:        Analog  
 REF:         Analog

#### 2. Outputs

RP OUT:     Analog  
 RMP:        Bit

#### 3. Implementation

The following holds true while the HLD, ZERO bits are set high and the RES bit is low (explained in detail in ADDITIONAL CONTROL I/O).

If REF is increasing faster than UP, the RMP bit is set high and RP OUT ramps at the UP value (time period  $t_1$  to  $t_2$  of Figure 4-61). If REF decreases faster than DWN, the RMP bit is set high and RP OUT ramps at the DWN value (time period  $t_3$  to  $t_4$  of Figure 4-61). If neither of the preceding conditions is true, the RMP bit is set low and RP OUT equals REF.

## RATE OF CHANGE LIMIT BLOCK

### 1. Inputs

INP:            Analog (Internally connected to the Ramp Output)  
RND:            Analog

### 2. Outputs

OUT:            Analog

### 3. Implementation

The rate of change limit block (ROC filter) is internal to the RMP2 Control Block. The purpose of this stage of the RMP2 block is to round the corners created by the ramp change block (Figure 4-61B). The ROC filter produces rounding by limiting the ramp rate of the input to the output over time. The limiting occurs as a result of a calculated value internal to the RMP2 called the Maximum Rate of Change. When the input is greater than the Maximum Rate of Change value, the output equals the Maximum Rate of Change value. When the Maximum Rate of Change equals the rate of the input, the ROC stops limiting the output.

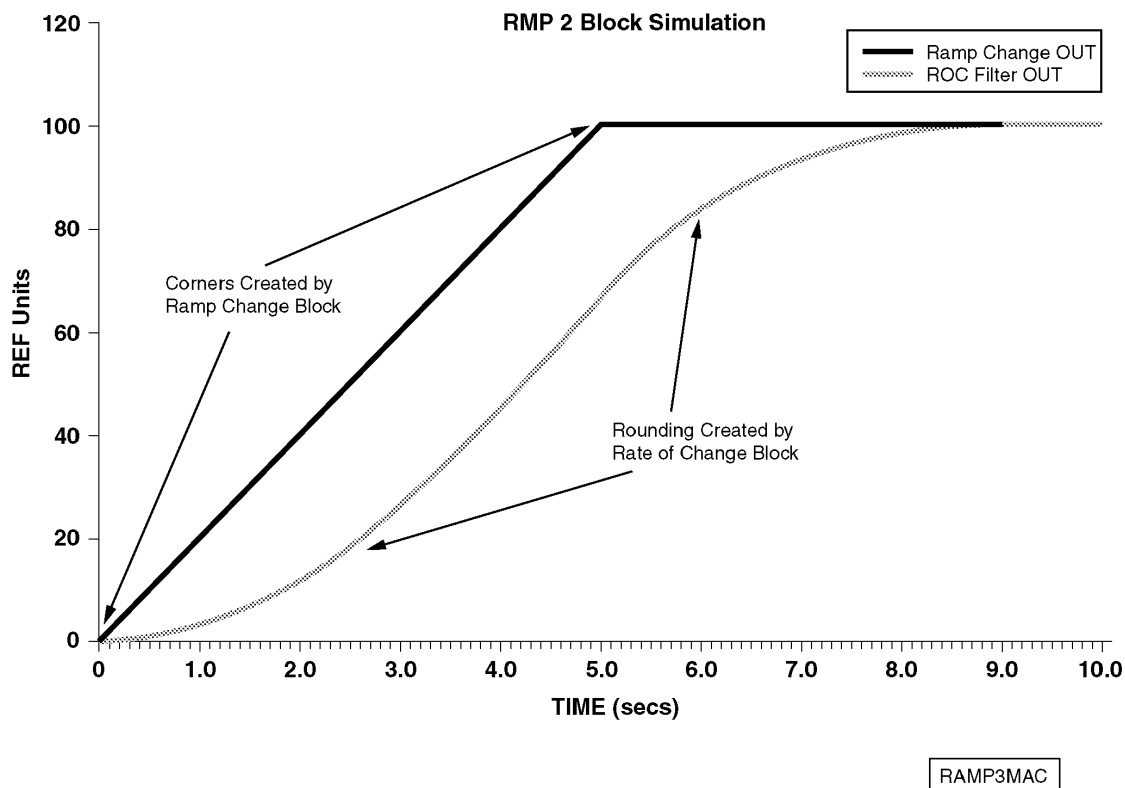


FIGURE 4-61B

The maximum rate of change allowed by the RMP2 ROC filter block depends upon time. This time is measured from the beginning of a ramp input to the present time instant. The maximum rate of change of the output of this filter is time dependent of the form:

$$\text{Rate} = S * T$$

Equation 4-61.1

where S is the analog value RND (units/Sec.<sup>2</sup>), and T (Sec.) is the point in time since the start of the ramp input. The maximum rate of change of the filter output will not exceed that of the input over a long enough time interval.

As an example, note on Figure 4-61B that the plot starts at time t = 0 Sec. The rate of change at the input of the filter block is a constant 20 FPM/S. The filter limits the rate of change block to 5FPM/Sec<sup>2</sup> thus:

Exact Time	ROC Filter (Slope) at OUT
1 Sec.	5 FPM/SEC
2 Sec.	10 FPM/SEC
3 Sec.	15 FPM/SEC
4 Sec.	20 FPM/SEC
5 Sec.	20 FPM/SEC

Notice that since the input to the filter is 20.0 FPM/SEC, the rate from 4 to 5 Sec. of the output does not increase past 20 FPM/SEC.

At 5 seconds, the Rate Change block reaches its final value (100 FPM) and the rate of change becomes zero. The filter will now cause the output rate to decrease by 5 FPM/SEC<sup>2</sup> from its maximum value of 20FPM/S while the input rate is zero, thus:

Exact Time	Maximum rate of change (Slope)
1 Sec.	5 FPM/SEC
2 Sec.	10 FPM/SEC
3 Sec.	15 FPM/SEC
4 Sec.	20 FPM/SEC
5 Sec.	20 FPM/SEC
6 Sec.	15 FPM/SEC
7 Sec.	10 FPM/SEC
8 Sec.	5 FPM/SEC
9 Sec.	0 FPM/SEC
10 Sec.	0 FPM/SEC

To accurately select an appropriate value for the RND input, apply Equation 4-61.1 in the form:

$$S = \text{Rate}/T$$

Where:

S = Value of Analog input RND

Rate = Value of UP or DWN.

T = Desired time length for ROC to provide rounding

**Equation 4-61.2**

ADDITIONAL CONTROL I/O1. Inputs

$\overline{\text{ZERO}}$	Bit
$\overline{\text{HLD}}$	Bit

2. Outputs

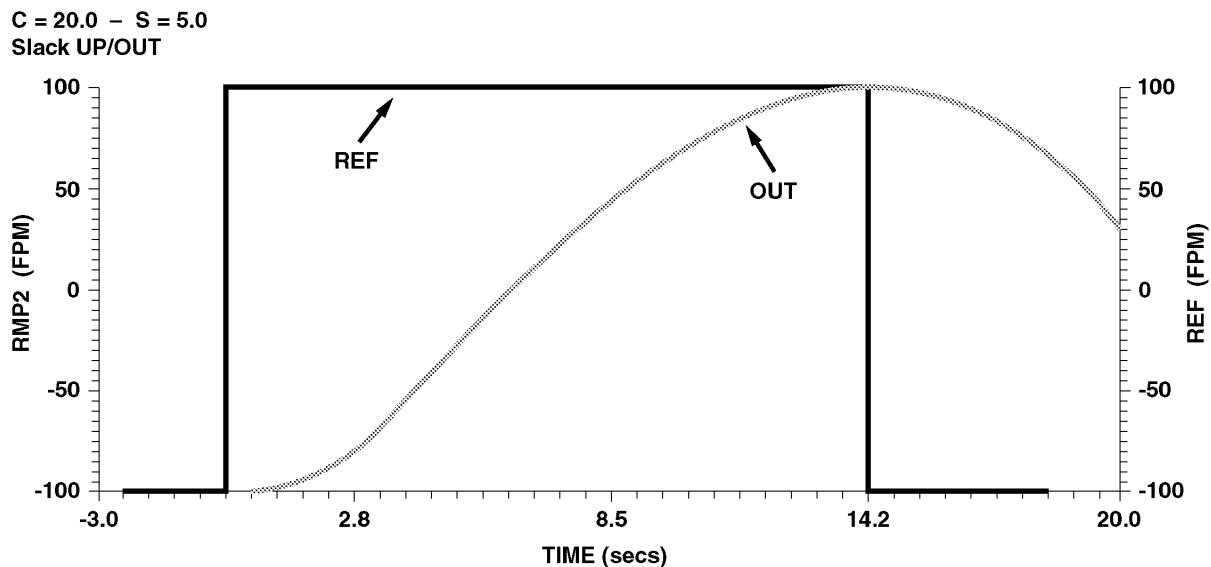
RES	Bit
-----	-----

If  $\overline{\text{ZERO}}$  bit is low,  $\text{OUT} = 0$ . When  $\overline{\text{ZERO}}$  bit goes high,  $\text{OUT}$  ramps to  $\text{REF}$  by the UP or DWN ramp rates in addition to the RND input.

If the RES bit is high,  $\text{OUT} = \text{REF}$ . (Second in priority)

If the  $\overline{\text{HLD}}$  bit is low,  $\text{OUT}$  is held at its present value. The rounding continues to prevent a step response. When  $\text{HLD}$  goes high,  $\text{OUT}$  ramps to  $\text{REF}$  by the appropriate rate.

The following figures 4-61C, 4-61D, and 4-61E graphically represent various RMP2 Control block input results.

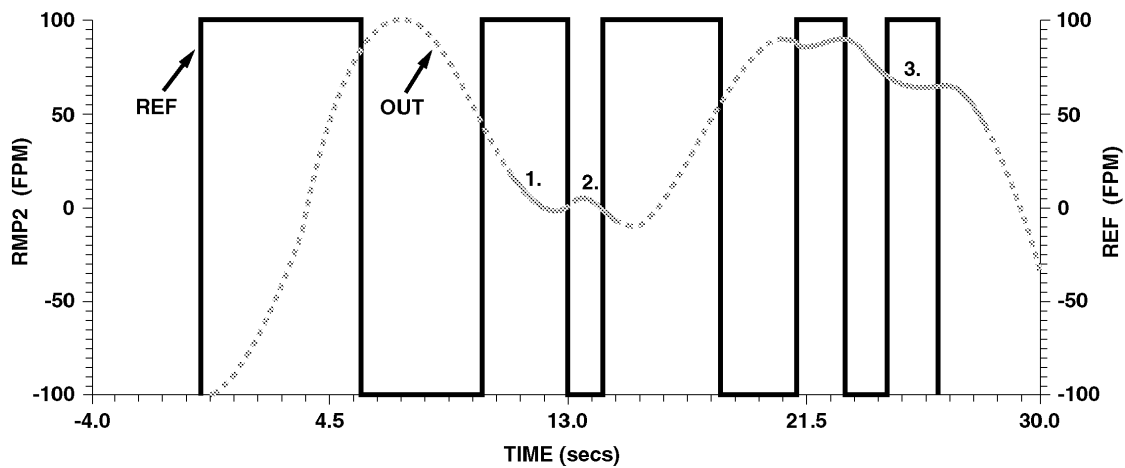


- RMP2 Ramps up and performs rounding to max value then switches to ramp and round negative to follow input.
- UP and DWN RATE 20 FPM/sec; RND = 5 FPM/sec<sup>2</sup>

RAMP4MAC

FIGURE 4-61C

C = 50 – S = 15  
Slack UP/OUT

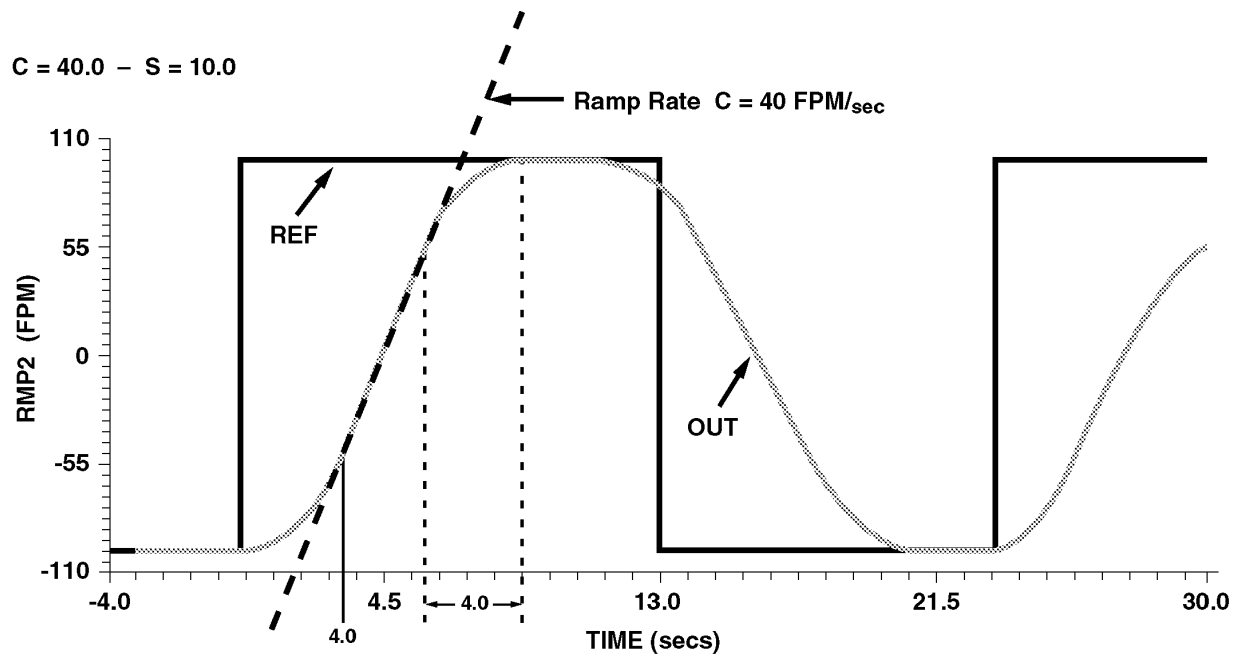


- 1.) RMP2 tries to turn around to follow the input while continuing to perform rounding.
- 2.) Easy transition from a small positive slope to change negative and follow input.
- 3.) RMP2 not very responsive to switching rates > RND

UP and DWN RATE = 50 FPM/sec; RND = 15 FPM/sec<sup>2</sup>

RAMP5MAC

FIGURE 4-61D



Calculation for S (where  $S = \text{RND}$  in  $\text{units/sec}^2$ )  
to obtain desired output, which is described below.

$$S = \frac{\text{RATE (Value of UP)}}{T \text{ (Chosen as 4 sec.)}} = \frac{40 \text{ FPM/sec}}{4 \text{ sec}} = 10 \text{ FPM/sec}^2$$

With a process that ramps up at a  $40 \text{ FPM/sec}$  rate, entering a SLCK SCURVE (RND; rounding rate) of  $10 \text{ FPM/sec}^2$ , will result in a starting and ending curve that takes 4 seconds to complete.

RAMP6MAC

FIGURE 4-61E



## 4.62 RRAMP3

The RRAMP3 block provides a variable rate linear ramp with user programmable smoothing. The purpose of this block is to provide a smooth reference from changing setpoint values.

The difference between the RRAMP3 block and RMP2 is the additional RAMP inputs. The RRAMP3 block has four ramp rates instead of two. See below.

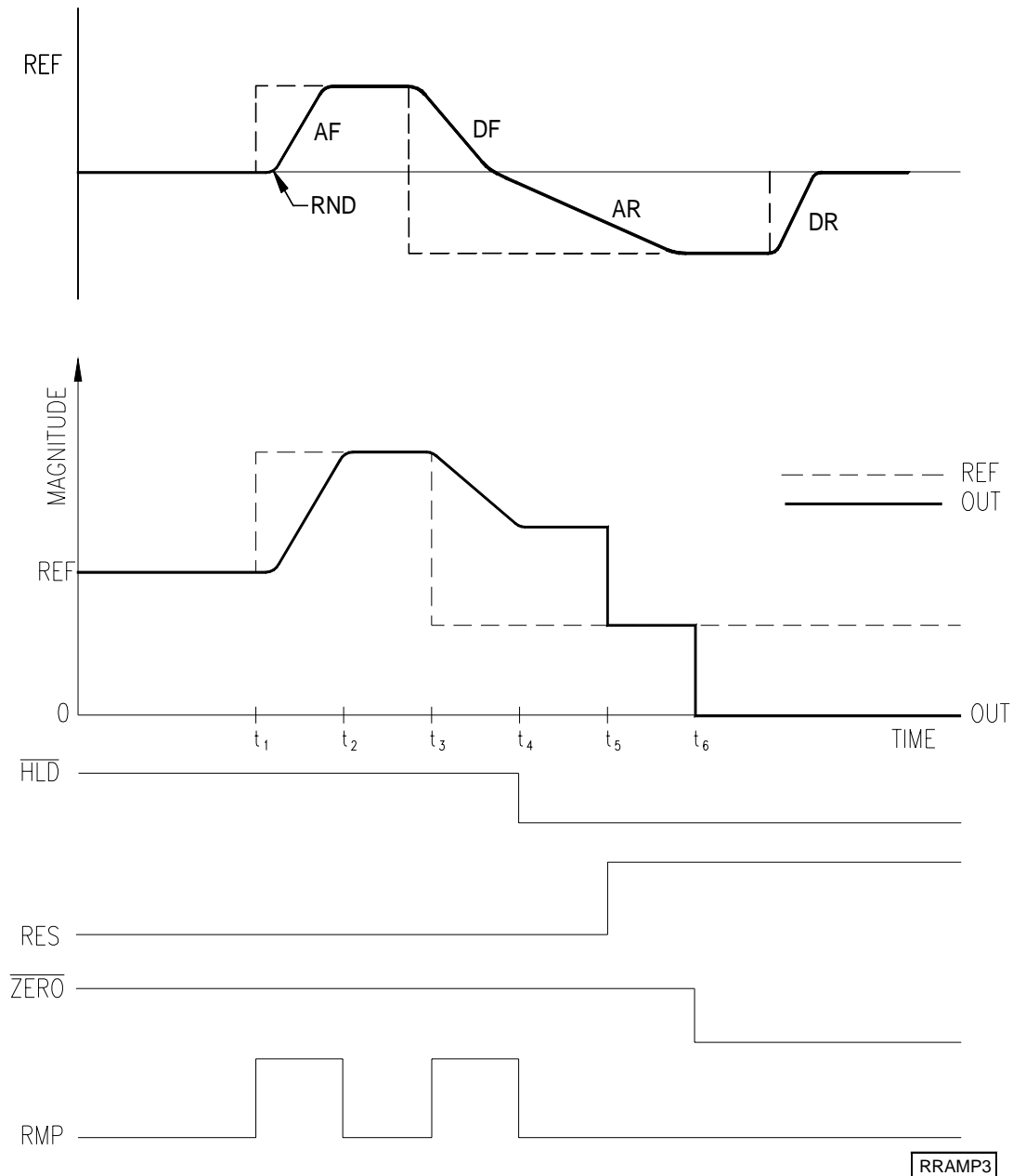


FIGURE 4-62. RRAMP3 BLOCK

The RRAMP3 block can be divided internally into three components to aid in the understanding of its operation. These components are a Ramp Change Block, a Rate of Change Limit Block and Additional Control I/O as can be seen in Figure 4-62A.

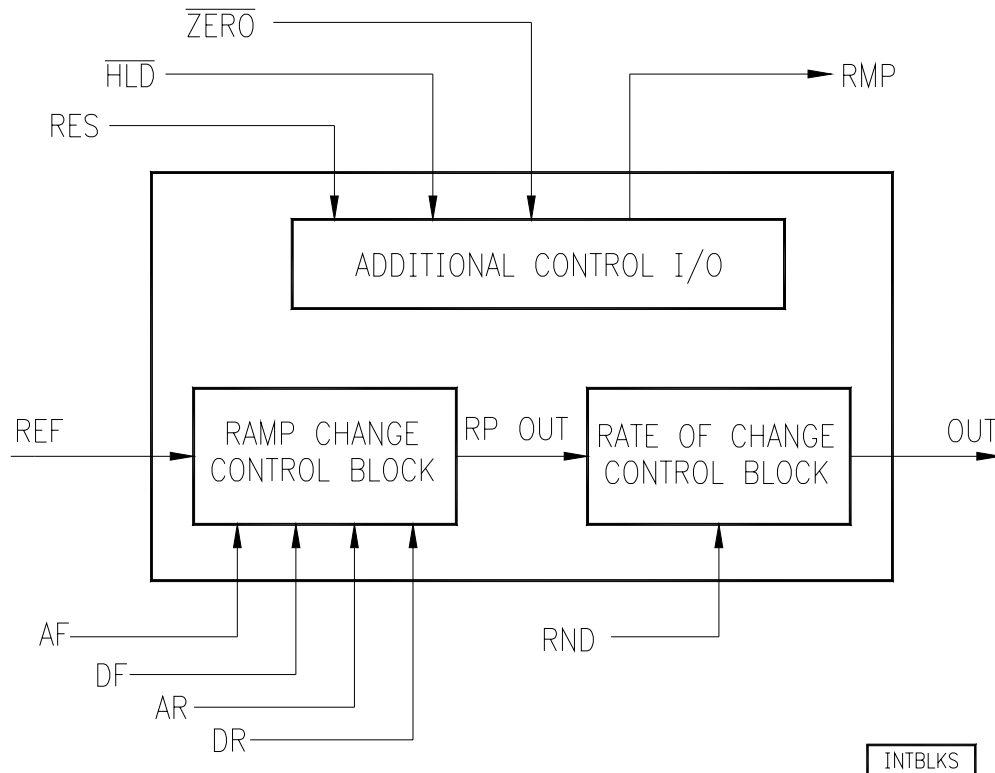


FIGURE 4-62A. INTERNAL CONTROL BLOCKS

### RAMP CHANGE BLOCK

#### 1. Inputs

REF: Analog  
 AF: Analog  
 DF: Analog  
 AR: Analog  
 DR: Analog  
 RND: Analog  
 RES: Digital

$\overline{\text{HLD}}$ : Digital

$\overline{\text{ZERO}}$ : Digital

## 2. Outputs

RP OUT:     Analog  
RMP:         Bit

## 3. Implementation

The following holds true while the HLD, ZERO bits are set high and the RES bit is low (explained in detail in ADDITIONAL CONTROL I/O).

If REF is increasing (positive) faster than AF, the RMP bit is set high and RP OUT ramps at the AF value (time period  $t_1$  to  $t_2$  of Figure 4-61). If AF is equal to zero, then the RP OUT ramps with REF. If REF decreases (but still positive) faster than DF, the RMP bit is set high and RP OUT ramps at the DF value (time period  $t_3$  to  $t_4$  of Figure 4-62). If DF is equal to zero, then the RP OUT ramps with REF. If neither of the preceding conditions is true, the RMP bit is set low and RP OUT equals REF. AR and DR work the same as AF and DF but are used when RP OUT becomes negative.

## RATE OF CHANGE LIMIT BLOCK

The rest of section 4.62 RRAMP3 is similar to the corresponding part of section 4.61 RMP2.

### 4.63 SBXDIA

The SBXDIA block calculates the diameter by relating a reference pulse generator with a once-per-revolution pickup. This block requires the GSBX board connected to the Maxi system board. The board provides the following:

- Reference pulse generator input
- (2) Once-per-revolution pickups
- (8) Definable digital inputs
- (4) Definable digital outputs

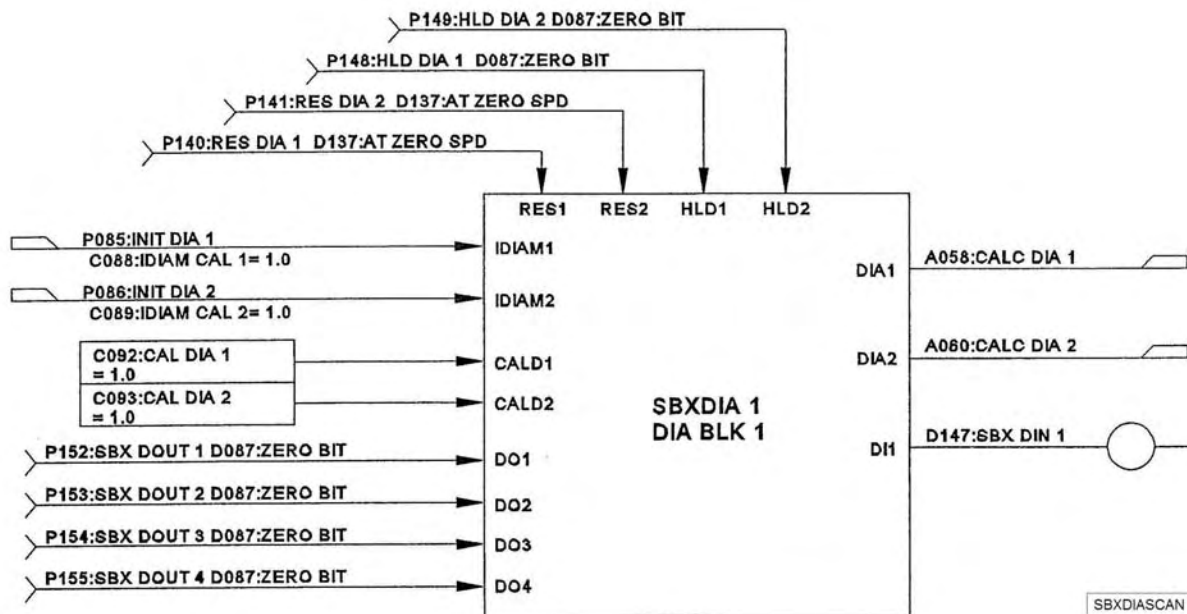


FIGURE 4-63. SBXDIA BLOCK

#### 1. Inputs

IDIAM1	Analog
IDIAM2	Analog
CALD1	Analog
CALD2	Analog
RES1	Digital
RES2	Digital
HLD1	Digital
HLD2	Digital

Inputs (Continued)

DO1	Digital
DO2	Digital
DO3	Digital
DO4	Digital

2. Outputs

DIA1	Analog
DIA2	Analog
DI1	Digital

3. Implementation

If the RES1 is high, then DIA1 = IDIAM1.

If HLD1 is high, the output is frozen at its last value. RES1 has a higher priority.

If RES1 and HLD1 are low, then DIA1 is calculated as follows:

$$\text{DIA1} = (\text{Edges read since last pickup reading}) * \text{CALD1/PI}$$

The first reading after a hold or reset is ignored by the block. This is to avoid a false diameter recording.

RES2, HLD2, DIA2, CALD2 work on the same principles.

DO1 through DO4 are the programmable digital outputs available on the board. These outputs must be isolated.

DI1 - First location where the eight digital inputs are stored. It will use the next seven locations to store the information.

4. Application Note

The GSBX board has the following hardware assignments for this block.

Pin 15 - Reference Frequency Input  
Pin 17 - Pick-up pulse 1  
Pin 4 - Pick-up pulse 2  
Pins 9, 13, 22 - Common

Additionally, this block can be used to calculate values other than diameter, by factoring out PI in the calibration number. One such use is for a length calculator, where product is metered and a proximity input resets when complete. The result is length.

#### 4.64 SBXDIA4

The SBXDIA4 block calculates the diameter by relating a reference pulse generator with a once-per-revolution pickup. This block requires the GSBX board connected to the Maxi system board. The board provides the following:

Reference pulse generator input  
 (4) Once-per-revolution pickups  
 (8) Definable digital inputs  
 (4) Definable digital outputs

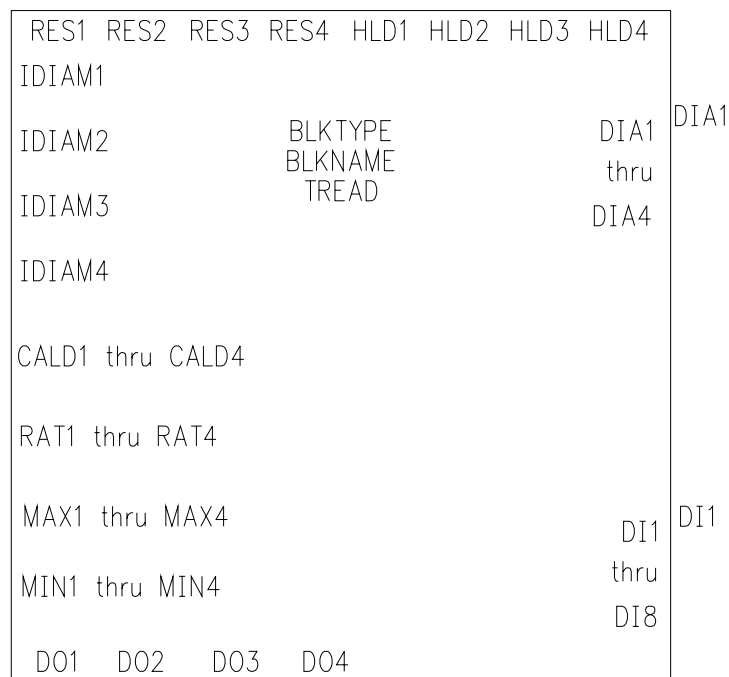


FIGURE 4-64. SBXDIA4 BLOCK

##### 1. Inputs

IDIAM1	Analog
IDIAM2	Analog
IDIAM3	Analog
IDIAM4	Analog
CALD1	Analog
RATE1	Analog
MAX DIA1	Analog
MIN DIA1	Analog

Inputs (Cont.)

RES1	Digital
RES2	Digital
RES3	Digital
RES4	Digital
HLD1	Digital
HLD2	Digital
HLD3	Digital
HLD4	Digital
DO1	Digital
DO2	Digital
DO3	Digital
DO4	Digital

2. Outputs

DIA1	Analog
DI1	Digital

3. Implementation

This block uses the GSBX board to generate four diameter readings. It does this by calculating the distance the material has traveled based on one revolution of the roll. The GSBX board has a pulse generator input to determine the distance and four inputs (one for each roll), which record once per revolution.

CALD1, RATE1, MAX DIA1, MIN DIA1, and DIA1 all point to the first diameter's parameters. The other three diameter parameters are in consecutive order.

If the RES1 is high, then DIA1 = IDIAM1.

If HLD1 is high, the output is frozen at its last value. RES1 has a higher priority.

If RES1 and HLD1 are low, then DIA1 is calculated as follows:

$$\text{DIA1} = (\text{Edges read since last pickup reading}) * \text{CALD1/PI}$$

The first reading after a hold or reset is ignored by the block. This is to avoid a false diameter recording.

RATE1 limits the rate of change of DIA1 when RES1 is not high. This is set in diameter process units per second.

DIA1 is limited to be within MAX DIA1 and MIN DIA1. This is also true while RES1 is active.

DO1 through DO4 are the programmable digital outputs available on the board. These outputs must be isolated.

DI1 is the first location where the eight digital inputs are stored. The next seven locations store the next seven inputs.

#### 4. Application Note

The GSBX board has the following hardware assignments for this block.

Pin 15 - Reference Frequency Input

Pin 17 - Pick-up pulse 1

Pin 4 - Pick-up pulse 2

Pin 16 - Pick-up pulse 3

Pin 3 - Pick-up pulse 4

Pins 9, 13, 22 - Common

DIN1 - Pin 21

DIN2 - Pin 8

DIN3 - Pin 20

DIN4 - Pin 7

DIN5 - Pin 19

DIN6 - Pin 6

DIN7 - Pin 18

DIN8 - Pin 5

DOUT1 - Pin 12

DOUT2 - Pin 24

DOUT3 - Pin 11

DOUT4 - Pin 23

Additionally, this block can be used to calculate values other than diameter. To do this, factor out PI in the calibration number. One such use is for a length calculator, where product is metered and a proximity input resets when complete.



#### 4.65 SDS SHEETS DURING STOP

This block calculates the number of sheets to be cut during a controlled stop (SDS). When using the AUTO STOP\* option, the number of sheets entered by the operator is subtracted from the number of sheets cut during the stop. When the selected number of sheets has been cut, the line will automatically begin to ramp to a stop. The line will stop after cutting the selected number of sheets.

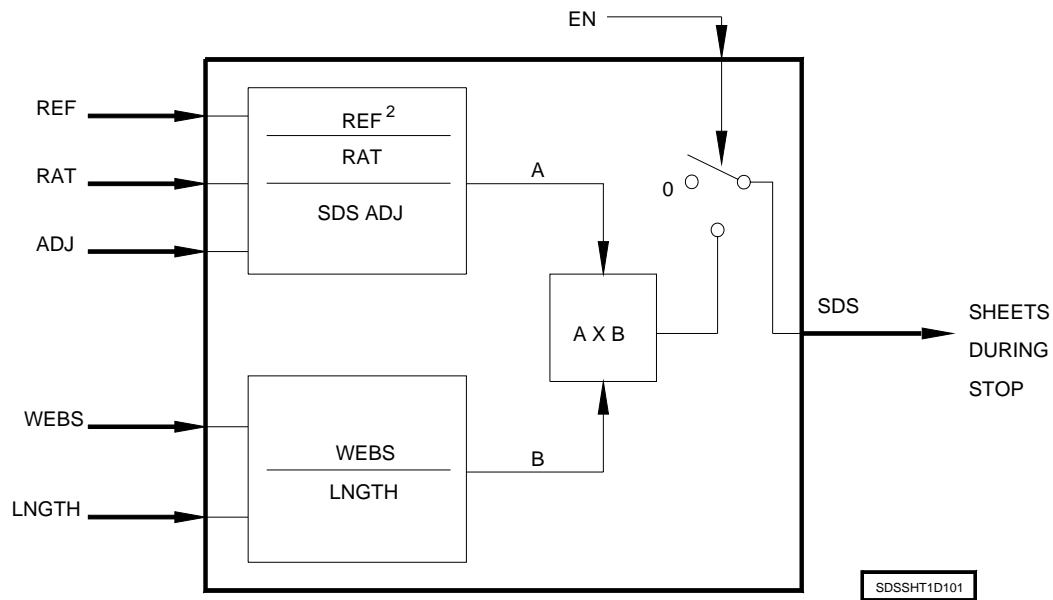


FIGURE 4-65. SDS SHEETS DURING STOP BLOCK

##### 1. Inputs

REF:	Analog
RAT:	Analog
ADJ:	Analog
WEBS:	Analog
LNGTH:	Analog
EN:	Digital

\* This function is not part of the ADDvantage-32 but is part of relay logic.

2. Outputs

SDS:            Analog

3. Implementation

If EN is high:

$$SDS = \frac{(REF^2) \times WEBS}{RAT \times ADJ \times LENGTH}$$

Where:

RAT = line speed in units per second

$$ADJ = \frac{(2)(60)**}{(CUT LENGTH UNITS \div LINE SPEED UNITS)} = 10$$

Else:

$$SDS = 0$$

- \*\*      60 =    60 seconds/1 minute to adjust stopping rate in seconds and line speed in minutes.  
           2 =    the factor used to obtain the integral number of sheets during the ramped stop.

## 4.66 SETPOINT

The Setpoint block enables the use of the INC and DEC inputs to modify a setpoint. The rates for the INC/DEC are adjustable along with the limits. The limits can be defined as min/max difference or ratio draw. This block is used in the beginning of the speed loop and tension loop.

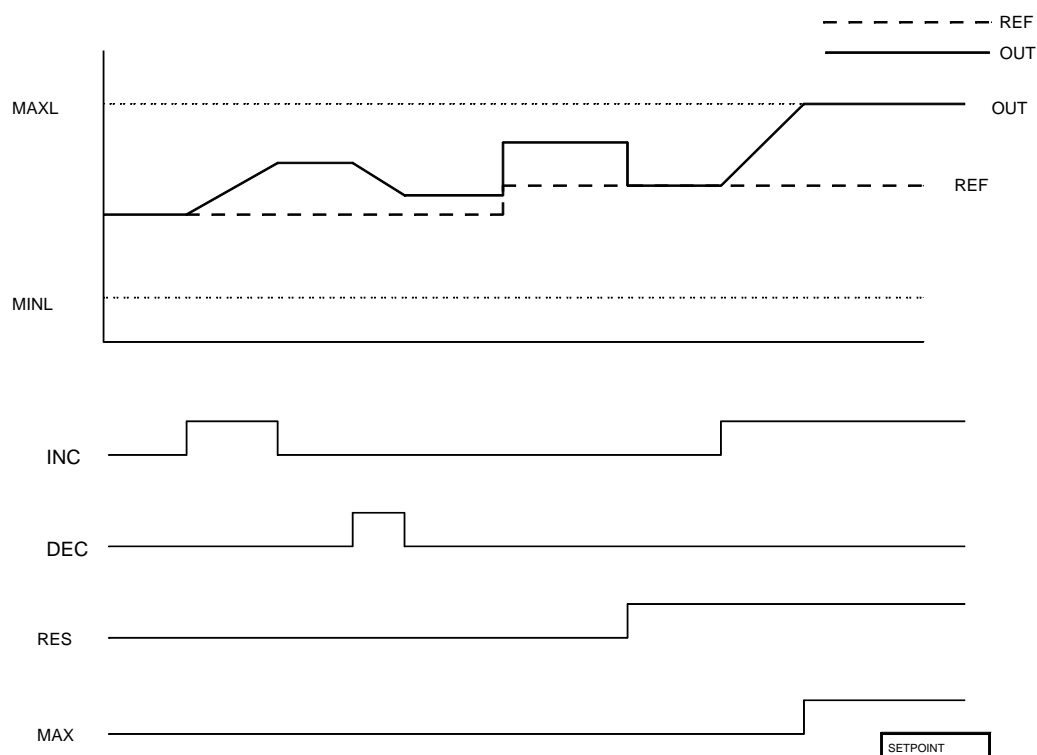


FIGURE 4-66. SETPOINT BLOCK

### 1. Inputs

REF:	Analog
RES:	Bit
INC:	Bit
DEC:	Bit
INCR:	Analog
DECR:	Analog
MAXL:	Analog
MINL:	Analog
ABS:	Bit
UP:	Bit
RET:	Bit

## 2. Outputs

OUT: Analog  
 DIF: Analog  
 MAX: Bit  
 MIN: Bit

## 3. Implementation

When the INC bit is high, the OUT value starts to ramp up at INCR rate. INCR is a rate entered in process units per second. The ramp continues until the INCR bit goes low or the OUT value reaches a limit. Upon reaching the limit, the MAX bit goes high and stays high until the OUT value goes below the limit. The limit is defined as follows.

If the ABS bit is low, the OUT value clamps at  $MAXL \times REF$ .

If the ABS bit is high, the OUT value clamps at  $MAXL + REF$ .

The DEC, DECR and MIN operate in the same manner as the INC functions.

If the UP input is high and REF changes, OUT will reset to equal REF and the INC/DEC changes will be negated.

If the UP input is low and REF changes, OUT changes depending on the ABS input. If the ABS bit is low, the OUT value changes by the REF value multiplied by the ratio of the INC/DEC change.

Example: ABS BIT = LOW

REF equals 100 and the INC bit is set high until OUT is increased to 150. Then if REF is changed to 200, OUT will equal 300.

$$\frac{(150)}{100} \times 200 = 300$$

If the ABS bit is high, the OUT value changes by the REF plus the INC/DEC change.

Example: ABS BIT = HIGH

REF equals 100 and the INC bit is set high until OUT is increased to 150. Then if REF is changed to 200, OUT will equal 250.

$$(150-100) + 200 = 250$$

On a low to high transition of the RES bit, OUT resets to the REF value.

DIF is equal to the change of the setpoint.

If ABS = 1, then DIF =  
OUT - REF (within the limits)

If ABS = 0, then  $DIF = \frac{OUT}{REF}$  (within the limits)

### RETENTIVE BLOCK

On powerup of the drive, OUT will be initialized under the following conditions:

If RET = 0 and ABS = 0,  
then DIF = 1 (within limits)

If RET = 0 and ABS = 1,  
then DIF = 0 (within limits)

If RET = 1, then DIF is not initialized.  
If ABS = 0, then  $OUT = INP \times DIF$ .  
If ABS = 1, then  $OUT = INP + DIF$ .

If a retentive setpoint is desired, configure a retentive point Y\*\*\*:RET SETPT\* to DIF so it updates automatically upon powerup. Configure the RES input to a zero bit to prevent resetting the output to the REF value instead of the retentive value.

## 4.67 SNAPAVG

### 1. Inputs

INP:	Analog
TICS:	Analog
RES:	Bit
HLD:	Bit
RET:	Bit

### 2. Outputs

OUT:	Analog
TTL:	Analog
CNT:	Analog

### 3. Implementation

The SNAPAVG block is used to get an average of a value with a specific time frame. The block has two internal count values to enable the block to function on short windows or longer windows.

TICS is internally limited to positive whole numbers.

On power up if RET is High, then the internal Count2 and Sum2 is set equal to Outputs CNT and TTL. Otherwise they are set equal to zero. Also, internal Count1 and Sum1 is set to zero on powerup. All three outputs go to zero on powerup also.

When the RES bit is high, then both counters and sums are set equal to zero.

When the hold bit is high, both counters and sums are held at their current value.

If both RES and HLD are low, then:

Every time the block is executed, INP is added to the internal Sum1. Also, the internal value Count1 is incremented.

When Count1 is greater than TICS, then:

Sum2 = Sum1 / Count1

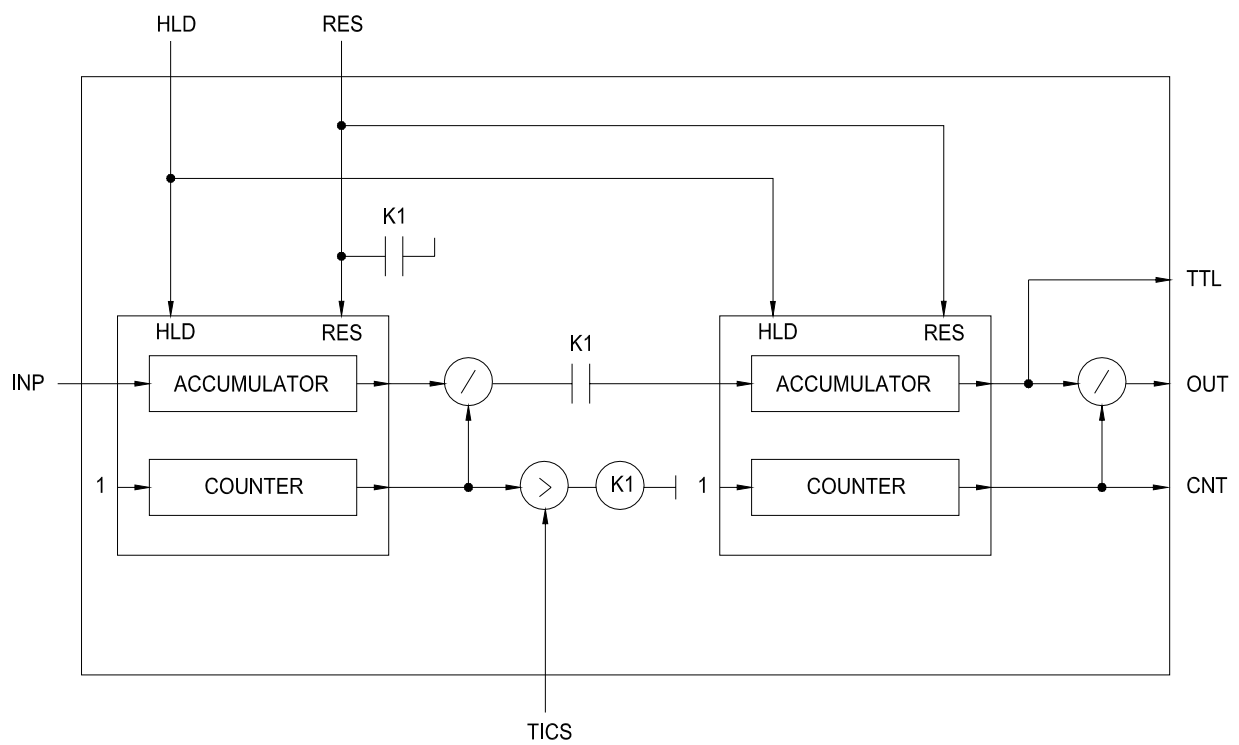
Count2 is incremented

Sum1 and Count1 is reset to zero.

OUT = Sum2 / Count2

TTL = Sum2

CNT = Count2



SNAPAVGLAN

FIGURE 4-67. SNAPAVG BLOCK

## 4.68 SPLICER

The Splicer block calculates two analog pulse count values, one for the pressure roll and one for the knife. Each value equals the amount of pulses to be received from the oncoming roll pulse generator before enabling the pressure roll and knife firing outputs.



FIGURE 4-68. SPLICER BLOCK

### 1. Inputs

PR T:	Analog	Pressure Roll Reaction Time (Sec)
KN T:	Analog	Knife Reaction Time (Sec)
TAIL:	Analog	Tail Length (Inches)
GR:	Analog	Gear Ratio for Oncoming Roll
PPR:	Analog	Tach PPR for Oncoming Roll
LGTH:	Analog	Static Length (Inches)
ON DIA:	Analog	Oncoming Roll Diameter (Inches)
GL A:	Analog	Glue Line Angle (Degrees)
CL A:	Analog	Clearance Angle (Degrees)
SPD R:	Analog	Speed Reference (FPM)

### 2. Outputs

PR F:	Analog	Pressure Roll Pulse Count Preset
KN F:	Analog	Knife Pulse Count Preset



3. Implementation

$$K = (PPR)(GR)$$

$$RPS = \frac{(SPD R)}{5\pi (ON DIA)}$$

$$PPS = K (RPS)$$

$$ANGLE = (RPS)(PR T)(360^\circ)$$

$$TMP = (GL A) - ANGLE$$

If  $TMP < 0.1$ ,  $TMP = TMP + 360^\circ$

Else,  $TMP = TMP + (CL A)$

$$PR F = K \left( \frac{TMP}{360^\circ} \right) \quad \text{Pressure Roll Firing Count}$$

$$TMP = PR F$$

$$TMP = TMP + [(PPS)(PR T)]$$

$$TMP = TMP + K \left( 1 - \frac{CL A}{360^\circ} \right)$$

$$TMP = TMP - (PPS)(KN T)$$

$$TMP2 = K \left[ \frac{TAIL - LGTH}{\pi (ON DIA)} \right]$$

$$TMP = TMP + TMP2$$

If  $TMP < 0$ ,  $TMP = TMP + K$

$$PR F = (PR F) + K$$

Else,  $KN F = TMP$  Knife Firing Count

#### 4.69 SUMMING JUNCTION, SELECTABLE 3 INPUT

This block adds input signals such as speed reference and tension trim. It selects which inputs to add using the bit select lines.

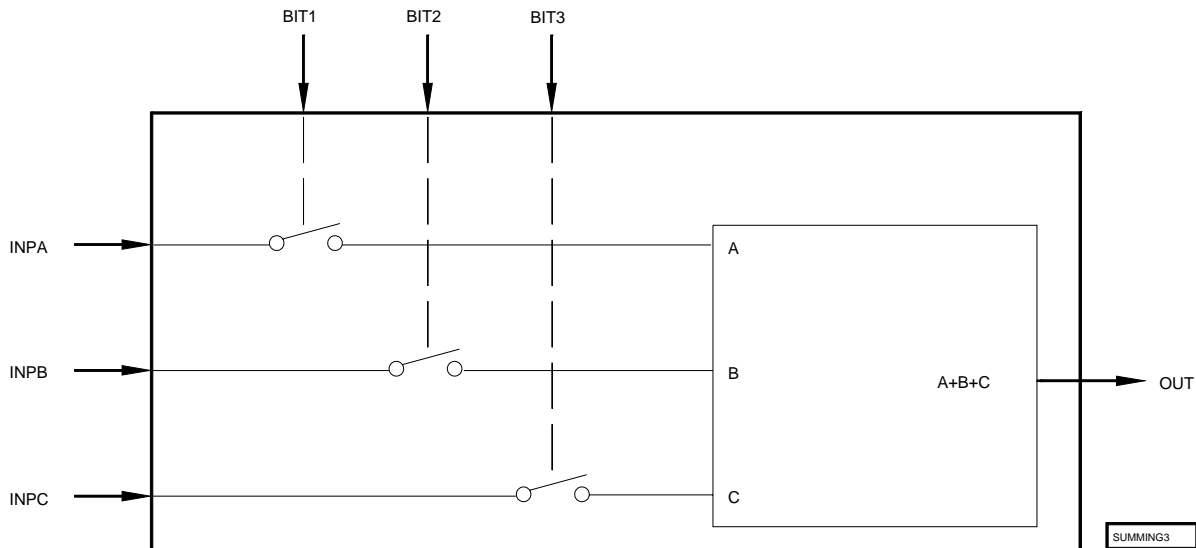


FIGURE 4-69. SUMMING BLOCK

##### 1. Inputs

INPA: Analog  
 INPB: Analog  
 INPC: Analog  
 BIT1: Bit  
 BIT2: Bit  
 BIT3: Bit

##### 2. Outputs

OUT: Analog

##### 3. Implementation

$$\text{OUT} = [(\text{INPA} \times \text{BIT1}) + (\text{INPB} \times \text{BIT2}) + (\text{INPC} \times \text{BIT3})]$$

If all 3 bits are low, then  $\text{OUT} = 0$ .

## 4.70 TABLE

The Table block is used to modify an analog variable "INP" by a factor which is proportional to a second analog variable "X\_IN". An example of such an application would be to taper a tension setpoint based on roll diameter.

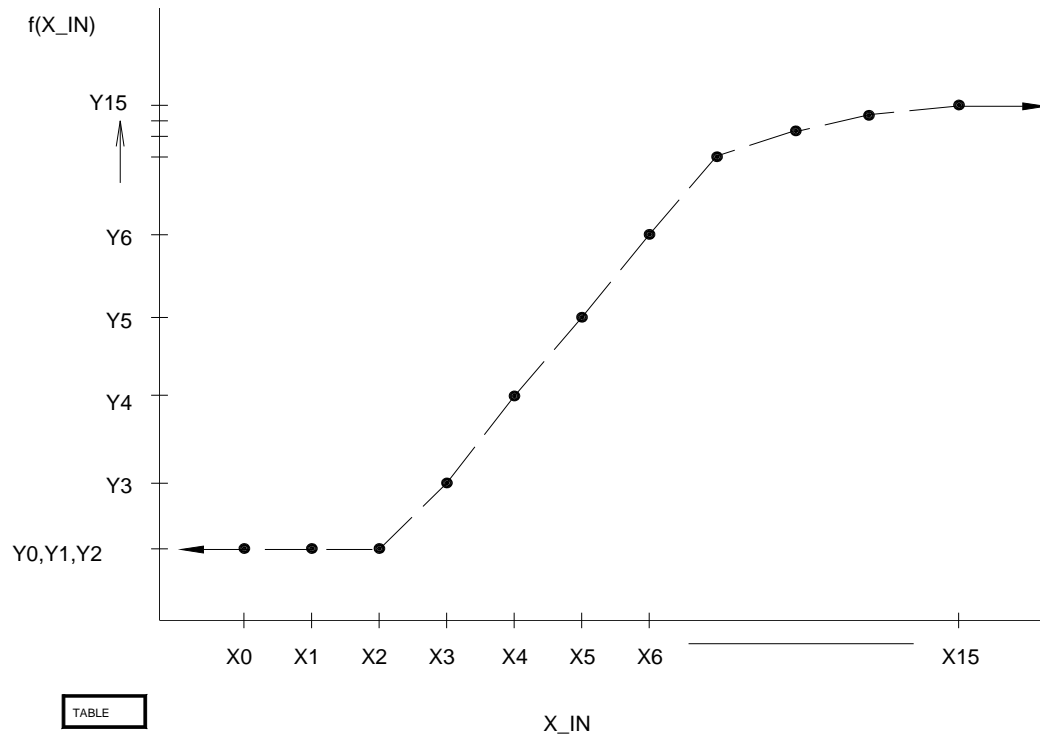


FIGURE 4-70. TABLE BLOCK

### 1. Inputs

INP: Analog  
 X\_IN: Analog  
 GAIN: Analog  
 TABLE: 0 - 3

### 2. Outputs

OUT: Analog

### 3. Implementation

The Table block is used to perform a non-linear look up operation  $y = f(X\_IN)$ , and output a value using the following formula:  $OUT = f(X\_IN) \times GAIN \times INP$ .

Where:

Y is calculated as a function of X\_IN by using the selected TABLE values.

A TABLE is defined as an array ( $2 \times 16$ ) in size, of x,y points where x values are entered in ascending order. (Refer to section 6.3.4, Tables Menu, for additional explanation.)

If X\_IN is less than the first X value in the TABLE, then  $f(X\_IN) =$  the first  $y_0$  value.

If X\_IN is greater than the last X value in the TABLE, then  $f(X\_IN) =$  the  $y_{15}$  point.

If X\_IN equals an X value in the TABLE, then  $f(X\_IN) =$  the y value associated with that X point.

If X\_IN falls between two X values in the TABLE, then  $f(X\_IN)$  is the interpolated between the two associated y values.

#### 4.71 TACH SELECT AND TACH SELECT-W

The blocks TACH SELECT and TACH SELECT-W are almost identical and behave as described below. The difference between the two blocks is described in the SPECIAL NOTE.

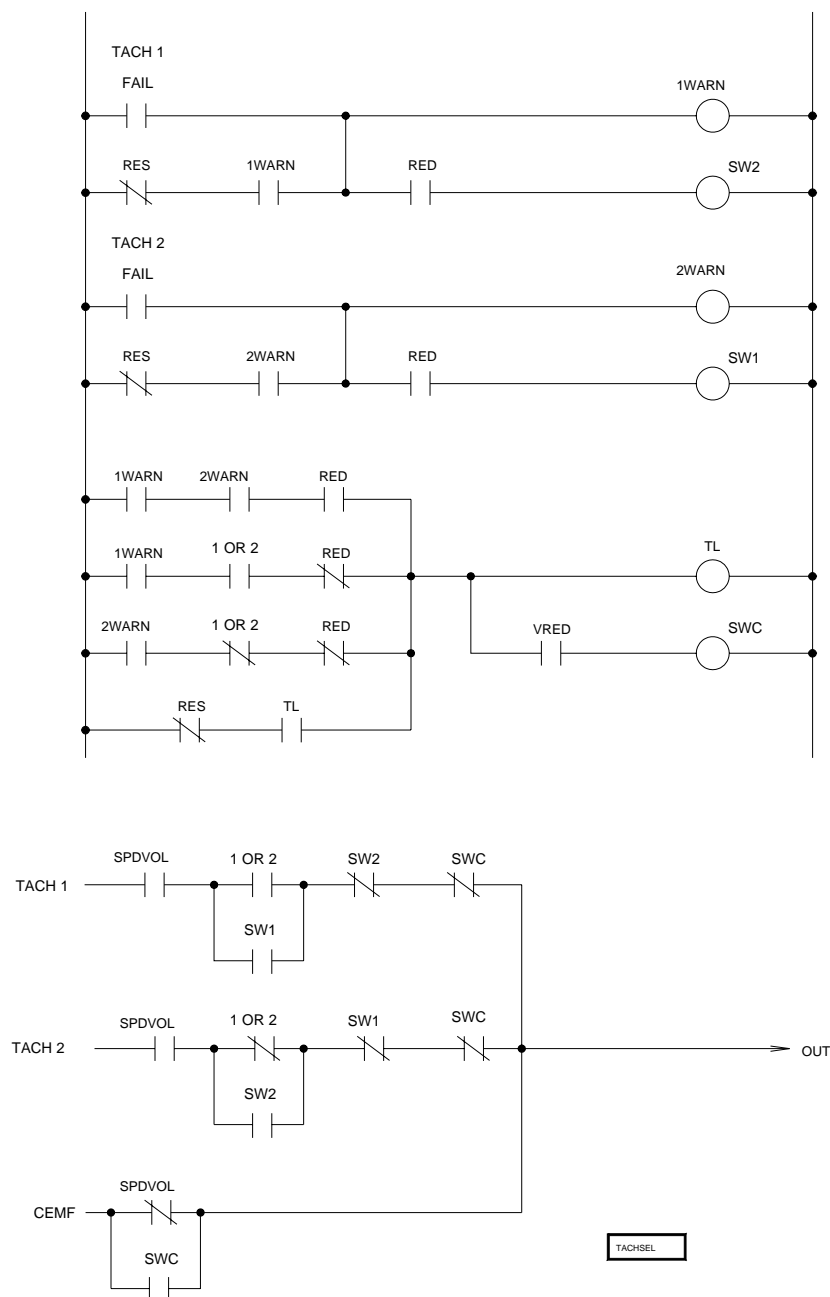


FIGURE 4-71. TACH SELECT AND TACH SELECT-W BLOCK

This block selects the type of speed feedback to be used by the speed loop. Either CEMF or speed feedback may be employed. When tach feedback is selected, tach loss detection can be used by configuring Y\*\*\*:USR FAULT 1 = TACH LOSS.

This block also has the option of using redundant tach inputs. On a tach loss of the primary tach, it can be specified to switch to a second tach feedback while still running the drive. If the tachs fail, CEMF feedback can be selected for the speed feedback. The tach inputs can be configured to either analog or digital feedbacks.

1. Inputs

TACH1:	Analog
TACH2:	Analog
CEMF:	Analog
MXSPD:	Analog
GAIN:	Analog
SPDVOL:	Bit
1 OR 2:	Bit
V RED:	Bit
RED:	Bit
RES:	Bit

2. Outputs

OUT:	Analog
1WARN:	Bit
2WARN:	Bit
TL:	Bit

3. Implementation

The speed output of the TACH SELECT block is selected from CEMF, TACH1, or TACH2 inputs, and scaled by the GAIN input. In order to work properly, the CEMF, TACH1, and TACH2 inputs need to be properly scaled into the appropriate units. If TACH feedback is scaled in FPM or other process units, the motor's CEMF input will need to be scaled into the identical units. Note: If frequency inputs are used as TACH input, Section III gives details on how the scaling parameters need to be set in order to get the proper units. The GAIN input can be used to scale all inputs into process units that will match the Speed Reference. Typical operation of the TACH SELECT block is described below.

If SPDVOL = low,  $OUT = CEMF \times GAIN$ .

If SPDVOL = high and 1 OR 2 = high, and no tach loss is detected,  
 $OUT = TACH1 \times GAIN$ .

If SPDVOL = high and 1 OR 2 = low, and no tach loss is detected,  
 $OUT = TACH2 \times GAIN$ .

Tach failure conditions are detected by comparing CEMF to TACH inputs as follows:

If  $CEMF \times GAIN > 0.20 \times MXSPD$  and  
 $TACH \times GAIN < 0.05 \times MXSPD$ ,

or If  $CEMF \times GAIN > 0.20$  and the polarity of CEMF  
 $\neq$  the polarity of TACH,

then tach failure will be detected regardless of whether the associated tach input is selected or not. Therefore, if CEMF feedback is used as the speed feedback, TACH LOSS should not be configured to a USR FAULT. Any time a tach failure is detected, the associated WARN bit will turn on. (That is, if a TACH1 failure is detected, the 1WARN bit turns on; if a TACH2 failure is detected, the 2WARN bit is turned on.)

If tach feedback is used (SPDVOL = high), and if a tach failure is detected, then the TACH SELECT block can be configured to automatically switch to the redundant tach or to control in CEMF. The logic is described in Figure 4-68 and as follows:

If SPDVOL = high and RED = high, then if a tach failure is detected, the output will switch from the failed tach to the redundant tach. For example, if 1 OR 2 = high, and the TACH1 input fails, OUT will switch from  $TACH1 \times GAIN$  to  $TACH2 \times GAIN$ .

If SPDVOL = high and V RED = high, then if a tach failure is detected, the output will switch from the failed tach feedback to CEMF feedback. For example, if 1 OR 2 = high, and the TACH1 input fails, OUT will switch from  $TACH1 \times GAIN$  to  $CEMF \times GAIN$ .

If SPDVOL = high and both RED and V RED = high, then if a tach failure occurs, the TACH SELECT block will switch first to the redundant tach; if the redundant tach fails, the output will switch to CEMF feedback.

\*\*\*\*\*

## WARNING

If SPDVOL = high and no redundancy is selected (both RED and V RED = low), then if a tach failure is detected in the primary tach, the TL bit will turn on, and the output will not switch from the failed tach. Similarly, if RED = high, but V RED = low, and if both tachs fail, the TL bit will turn on and the output will not switch but will remain dependent on the failed tach. In such a situation, a tach failure could cause equipment to "run away" and damage machinery or injure personnel. For this reason, any time V RED = low and SPDVOL = high, Avtron HIGHLY RECOMMENDS configuring one of the USR FAULTS (described in Section III) to the TL output of the TACH SELECT block.

\*\*\*\*\*

Any time a tach failure is detected, the TACH SELECT block will set appropriate output bits, and switch speed feedback as the logic requires. The outputs will remain in their states until the RES turns on. If the RES input is maintained in the high state, the TACH SELECT block will not switch to any redundant modes, and tach failures will not be detected.

### SPECIAL NOTE:

The TACH SELECT block differs from the TACH SELECT-W block in how the GAIN input is used to scale input feedback. The TACH SELECT block scales all inputs (TACH1, TACH2, and CEMF) and compares the scaled inputs to the MXSPD input to determine tach failures (i.e., tach fail is sensed if  $CEMF \times GAIN > 0.2 \times MXSPD$  and  $TACH \times GAIN < 0.05 \times MXSPD$ ). The TACH SELECT-W block compares the unscaled inputs to MXSPD in determining tach failures (i.e., tach fail is sensed if  $CEMF > 0.2 \times MXSPD$  and  $TACH < 0.05 \times MXSPD$ ). All other block operation and logic are identical.



## 4.72 TIMER

The Timer block is used to delay setting a bit until an appropriate count has occurred. It can be used to buffer faults for FIFO logging or to shut the drive down if in maximum tension for a period of time.

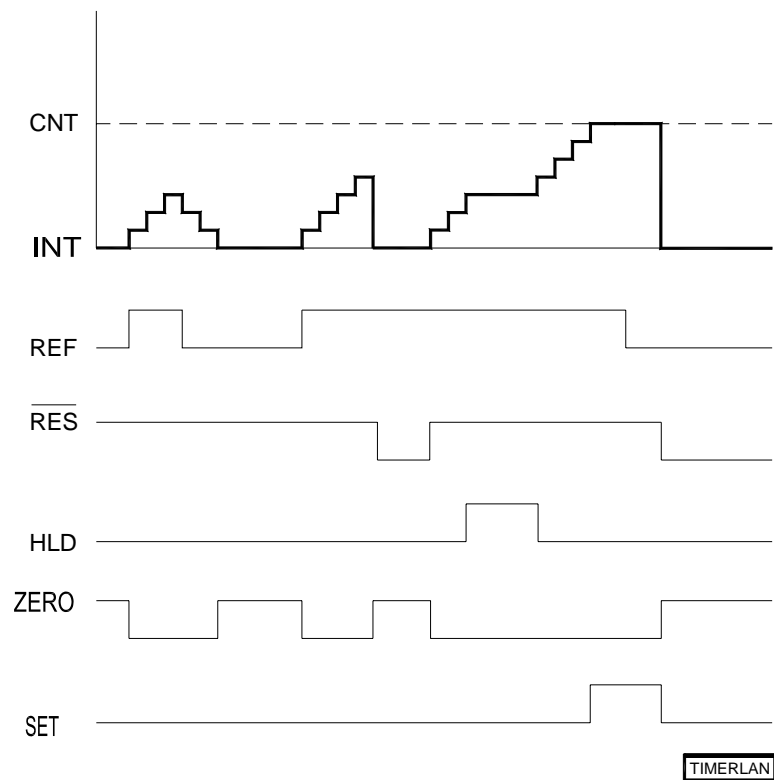


FIGURE 4-72. TIMER BLOCK

### 1. Inputs

HLD:	Bit
RES:	Bit
REF:	Bit
RET:	Bit
CNT:	Analog (1 - 1,000,000)

### 2. Outputs

SET:	Bit
ZERO:	Bit
VAL:	Analog

### 3. Implementation

When the RES bit equals zero, VAL is set to 0.

When VAL = 0, then ZERO bit = 1.

If VAL  $\neq$  0, then ZERO bit = 0.

When the HLD bit is high, VAL is frozen. The RES bit has higher priority than the HLD bit.

If RES = 1 and HLD = 0, then the following occurs:

If REF = 1 and VAL < CNT, then VAL = VAL + 1.

If REF = 0 and VAL > 0, then VAL = VAL - 1.

If VAL = CNT, then SET = 1, else SET = 0.

When SET = 1, it latches until a reset occurs.

#### Non-retentive Block

On powerup of the ADDvantage-32, VAL = 0

#### Retentive Block

On powerup of the ADDvantage-32, VAL will be initialized under the following conditions:

If RET = 0, then VAL = 0

If RET = 1, VAL is set to its last value prior to power loss. VAL must be configured to a retentive point Y\*\*\*:RET SETPT\* to be updated automatically on powerup.

### 4.73 TYPE 2 DIA

This block calculates the roll diameter of a center driven winder or unwinder section by using operator entered material thickness value and counting the number of spindle revolutions. This diameter calculation block can be used instead of the RATIO block. It is as accurate as the value of THCK that is entered. THCK is the average thickness of the material.

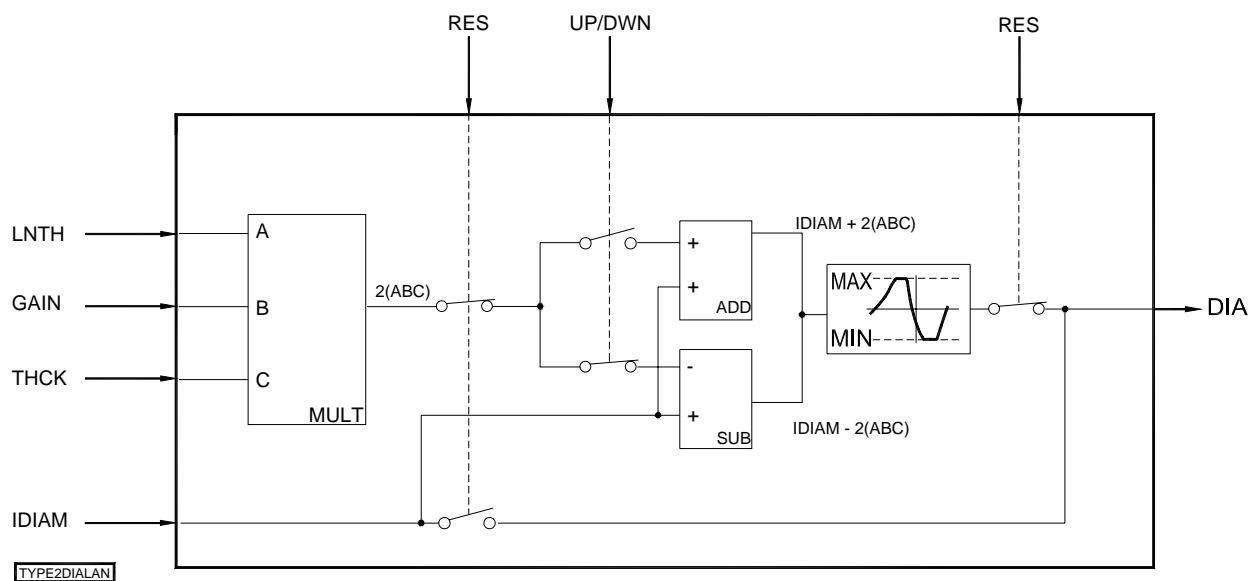


FIGURE 4-73. TYPE 2 DIA BLOCK

#### 1. Inputs

THCK:	Analog
IDIAM:	Analog
LNTH:	Analog
MAX:	Analog
MIN:	Analog
GAIN:	Analog
UP/DWN:	Bit
RES:	Bit

#### 2. Outputs

DIA:	Analog
------	--------

### 3. Implementation

If RES is high, then the output DIA = IDIAM.

If DIA is calculated to go beyond the MAX diameter or MIN diameter limits, then DIA will be clamped at the limit.

When the RES bit is set low, the DIA is calculated by the following:

If UP/DWN is high, then:

$$\text{DIA} = (\text{LNTH}/\text{GAIN} \times 2 \times \text{THCK}) + \text{IDIAM}$$

If UP/DWN is low, then:

$$\text{DIA} = \text{IDIAM} - (\text{LNTH}/\text{GAIN} \times 2 \times \text{THCK})$$

Length needs to be configured to the frequency counter from the winder tach. The counter needs to be reset at new roll.

Length divided by Gain should be equal to roll revolutions for the block to work properly.

#### 4.74 TYPE 3 DIA

This block calculates the roll diameter of a winder by counting the footage of the surface roll section. The accuracy of this block is comparable to the value of  $\text{THICK} + \text{DIA}$ . (THICK is the average thickness of the material.)

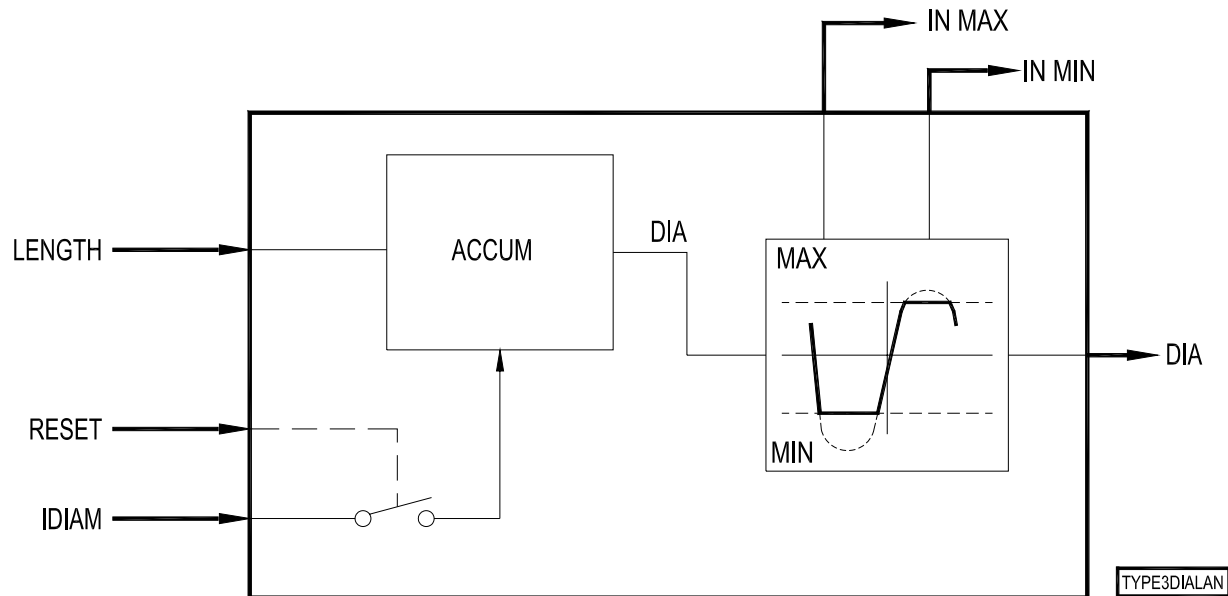


FIGURE 4-74. TYPE 3 DIA BLOCK

##### 1. Inputs

THICK:	Analog
IDIAM:	Analog
LENGTH:	Analog
MAX DIA:	Analog
MIN DIA:	Analog
UP/DWN:	Bit
RESET:	Bit
RET:	Bit

##### 2. Outputs

DIA:	Analog
IN MAX:	Bit
IN MIN:	Bit

### 3. Implementation

If RESET is set high, then DIA = IDIAM.

If DIA is calculated to exceed either the MAX DIA or MIN DIA limits, then DIA will be clamped at the limit and its corresponding output bit will go high.

For a winder system, set the UP/DWN bit high. The DIA increases by 2X THICK each time the following equation is true.

$$\text{LENGTH (New)} > \pi \times \text{DIA} + \text{Length (Old)}$$

For an unwinder system, set the UP/DWN bit low. DIA increases by 2X THICK each time the following equation is true.

$$\text{LENGTH (New)} > \pi \times \text{DIA} + \text{Length (Old)}$$

#### **NOTE**

LENGTH = Footage value of material from tach counters.

THICK = Average thickness of material (Entered in process units).

#### Non-retentive Block

On powerup of the ADDvantage-32, DIA = IDIAM

#### Retentive Block

On powerup of the ADDvantage-32, DIA will be initialized under the following conditions:

If RET = 0, then DIA = IDIAM

If RET = 1, DIA is set to its last value prior to power loss. DIA must be configured to a retentive point Y\*\*\*:RET SETPT\* to be updated automatically on powerup.

#### 4.75 UNITY SCALE

The Unity Scale block rescales the minimum and maximum limits of a given value to 0-1.

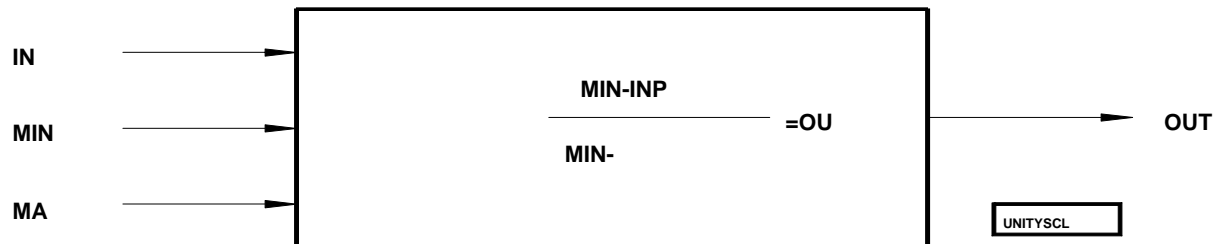


FIGURE 4-75. UNITY SCALE BLOCK

##### 1. Inputs

INP: Analog  
 MIN: Analog  
 MAX: Analog

##### 2. Outputs

OUT: Analog

##### 3. Implementation

If  $\text{MIN} - \text{MAX} \neq 0$ , then  $\text{OUT} = \text{MIN} - \text{INP} / \text{MIN} - \text{MAX}$ .  
 If  $\text{MIN} - \text{MAX} = 0$ , then  $\text{OUT} = 0$ .

## 4.76 UV PROTECT

The block can be used to try to prevent a shoot through condition on a low AC voltage. It does this by disabling the regenerating bridge current limit in a low voltage condition.

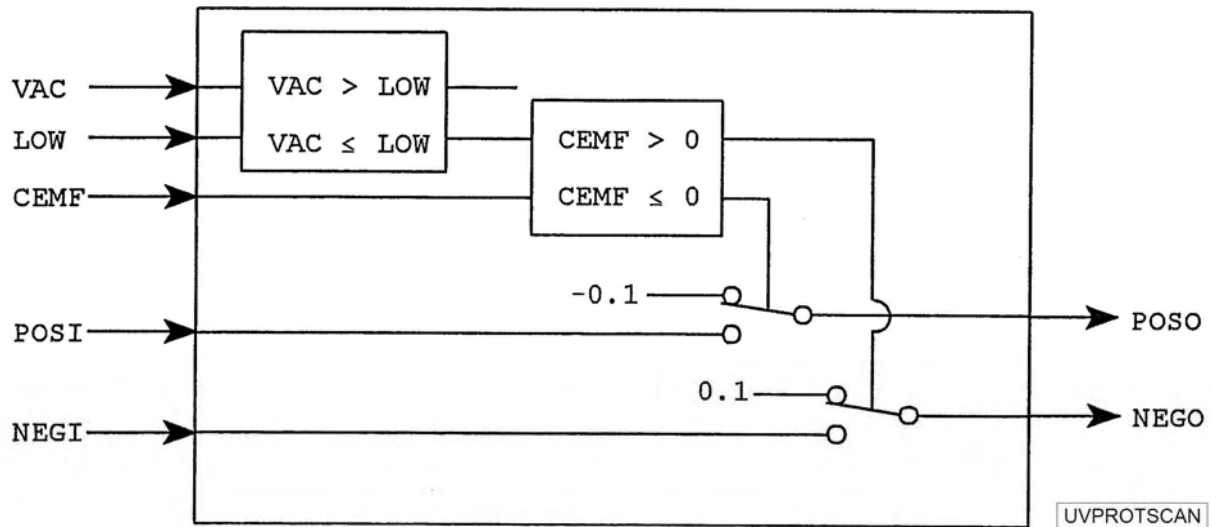


FIGURE 4-76. UV PROTECT BLOCK

### 1. Inputs

POSI: Analog  
 NEGI: Analog  
 VAC: Analog  
 LOW: Analog  
 CEMF: Analog

### 2. Outputs

POSO: Analog  
 NEGO: Analog

### 3. Implementation

If VAC is greater than the LOW input, then POSO = POSI and NEGO = NEGI.

Otherwise a low line condition is present and the following occurs.



If CEMF is Positive  
     $POSO = POSI$   
     $NEGO = 0.1\%$

If CEMF is Negative  
     $POSO = -0.1\%$   
     $NEGO = NEGI$

In the application, execute the block between the current limit setpoints and the current loop limit to protect the drive.

## 4.77 WINDER WK/D

This block calculates the inertia of a winder/unwinder. The inertia of the material which is essentially a hollow cylinder is equal to  $WK2 = \text{const} \times \text{width} \times ((\text{dia}^4) - (\text{core dia}^4))$ . Therefore, total inertia of a roll of material is the result of the previous equation plus the fixed inertia.

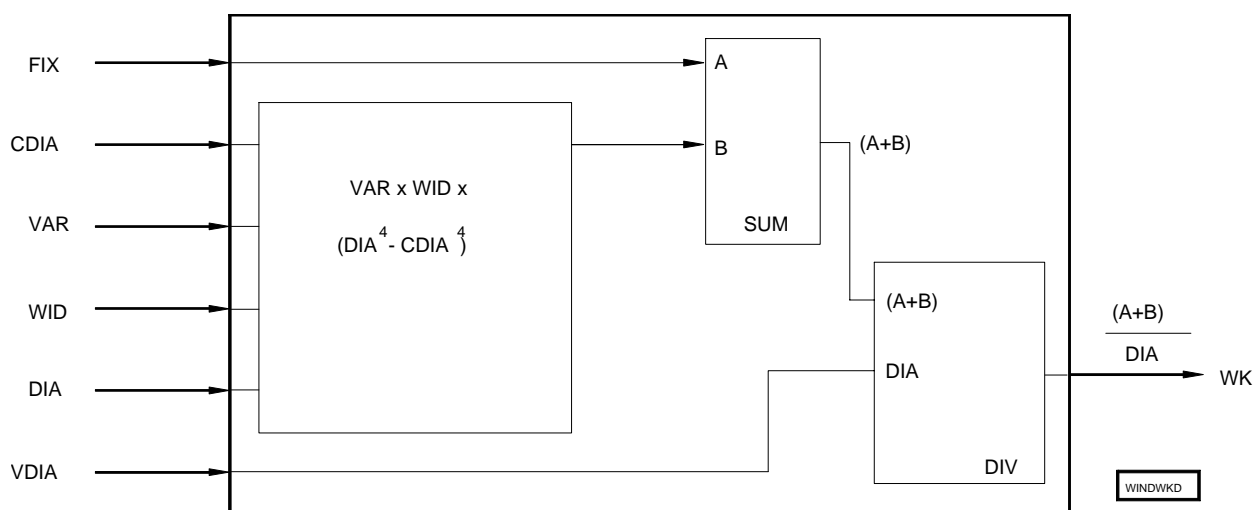


FIGURE 4-77. WINDER WK/D BLOCK

### 1. Inputs

VAR: Analog  
 WID: Analog  
 DIA: Analog  
 FIX: Analog  
 CDIA: Analog  
 VDIA: Analog

### 2. Outputs

WK: Analog

### 3. Implementation

$$WK = \frac{(\text{VAR})(\text{WID})(\text{DIA}^4 - \text{CDIA}^4) + \text{FIX}}{\text{VDIA}}$$

The torque required to accelerate a roll is equal to the  $WK^2$  of the body times the change in RPM.

$$\text{Torque} = WK^2 \times \frac{\text{Change in RPM}}{\text{Time}} \quad (\text{For a Fixed Diameter})$$

$$\text{Torque} = WK^2 \times \frac{\text{Change in FPM}}{\text{Time}} \quad (\text{For a Variable Diameter})$$

The D/DT block is used for  $\frac{\text{Change in FPM}}{\text{Time}}$ .

Therefore, the amount of current needed to accelerate a roll should equal the output of the WK/D block times the output of the D/DT block. This should be calculated for a core first (DIA = CDIA) and then a full roll of material (CDIA = MAXIMUM DIAMETER).

## 4.78 WINDOW COMPARE

The Window Compare takes an input and checks to see if it is between a high and low setpoint. The block offers options for absolute value of the input and a complementary output bit.

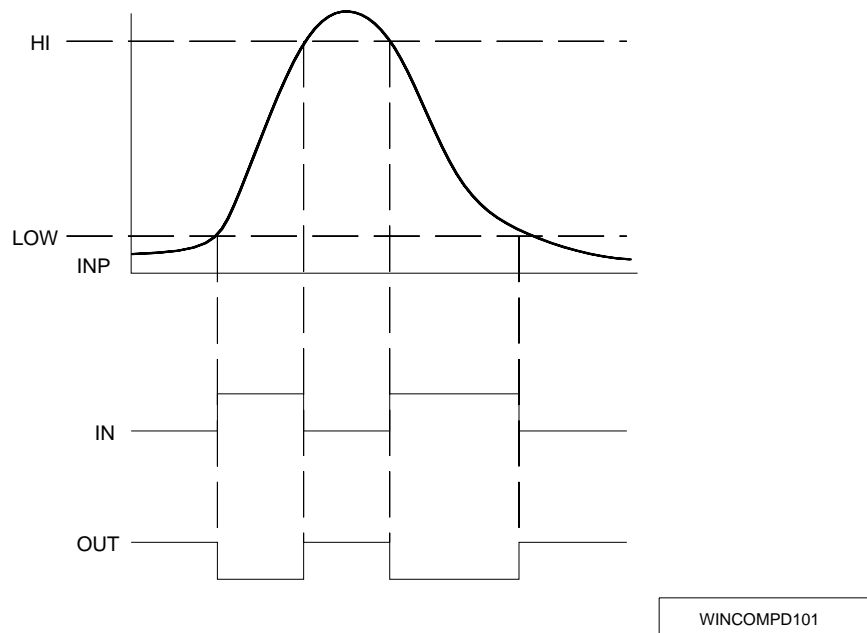


FIGURE 4-78. WINDOW COMPARE BLOCK

### 1. Inputs

INP:	Analog
HI:	Analog
LOW:	Analog
ABS:	Digital

### 2. Outputs

IN:	Digital
OUT:	Digital

### 3. Implementation

If ABS is Low (0), then

IN = 1 if (LOW <= INP <= HI)

Else IN = 0.

If ABS is High (1), then

IN = 1 if (|LOW| <= |INP| <= |HI|)

Else IN = 0.

If IN = 1    OUT = 0

Else IN = 0    OUT = 1



## SECTION V

# SIGNAL ANALYZER

The signal analyzer is a four-channel memory recorder capable of recording both digital and analog information. Each channel has separate setup and trigger parameters, allowing any information in the analog and digital tables to be recorded. After the information is captured, it can be directed to an analog output, displayed on the LCD display or uploaded to the human interface module.

Setup of the signal analyzer is accomplished using the Z\*\*\* parameters. These parameters consist of both calibration and configuration parameters which perform the following functions:

1. Data Collection
2. Channel Triggering
3. Sample Rate
4. Preview
5. Arming
6. Channel Enable
7. Channel Reset

The signal analyzer has 16K bytes of RAM. Each data point requires 4 bytes of RAM, allowing 1,000 points of information to be stored for each channel. If power is lost, all information captured by the analyzer is lost.

Specific parameter numbers have been omitted and replaced with asterisks due to differing parameter numbers between software. Consult Appendices A-D for exact parameter numbers and descriptions.

## 5.1 DATA COLLECTION

The data stored in the recorder channels can be any analog information or digital bit information located in the data tables. The recorder must be disabled to change the parameter. Defaults:

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:INP1 A/D Z***:INP1 ANALG Z***:INP1 DIG	Q***:ANALOG A***:IARM CMD D***:I-LIM LED
#2	Z***:INP2 A/D Z***:INP2 ANALG Z***:INP2 DIG	Q***:ANALOG A***:FLD CURRENT D***:RUNX
#3	Z***:INP3 A/D Z***:INP3 ANALG Z***:INP3 DIG	Q***:ANALOG A***:MOTOR CEMF D***:FWD BR LED
#4	Z***:INP4 A/D Z***:INP4 ANALG Z***:INP4 DIG	Q***:ANALOG A***:FLD CURRNT D***:REV BR LED

## 5.2 TRIGGER

Set for a rising edge or falling edge trigger, the recorder can be triggered from any analog or digital bit information located in the data tables. The recorder must be disabled to change these parameters. Default for all four recorders:

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:TRIG1 A/D Z***:TRIG1 ANALOG Z***:TRIG1 DIG Z***:TRIG R/F 1 Z***:TRIG LEVEL1	Q***:ANALOG A***:ACT SPEED D***:FAULT Q***:RISING 0.5



RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#2	Z***:TRIG2 A/D	Q***:ANALOG
	Z***:TRIG2 ANALOG	A***:ACT SPEED
	Z***:TRIG2 DIG	D***:FAULT
	Z***:TRIG R/F 2	Q***:RISING
	Z***:TRIG LEVEL2	0.5
#3	Z***:TRIG3 A/D	Q***:ANALOG
	Z***:TRIG3 ANALOG	A***:ACT SPEED
	Z***:TRIG3 DIG	D***:FAULT
	Z***:TRIG R/F 3	Q***:RISING
	Z***:TRIG LEVEL3	0.5
#4	Z***:TRIG4 A/D	Q***:ANALOG
	Z***:TRIG4 ANALOG	A***:ACT SPEED
	Z***:TRIG4 DIG	D***:FAULT
	Z***:TRIG R/F 4	Q***:RISING
	Z***:TRIG LEVEL4	0.5

### 5.3 SAMPLE RATE

The sample rate determines the time span between the recording of each data point. The rate is determined by specifying the number of 11.11 msec (for 60 Hz systems) time increments required between samples. For example, the shortest and longest sample times are:

Sample Time = Z\*\*\*:RATE X \* 11.11 msec

Range of Z\*\*\*:RATE X = (1 to 99,999)

Shortest Sample Time = (1) \* 11.11 msec = 11.11 msec

Longest Sample Time = (99,999) \* 11.11 msec = 1111 sec

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE	RANGE
#1	Z***:RATE 1	18 (200.00 ms).	1-99,999
#2	Z***:RATE 2	18	1-99,999
#3	Z***:RATE 3	18	1-99,999
#4	Z***:RATE 4	18	1-99,999

## 5.4 PREVIEW

Information recorded by the signal analyzer channels is broken into 1,000 individual points. When a particular channel is triggered, a preview can be set to show a number of samples before the trigger occurred. This allows information leading up to the trigger point to be evaluated. For example, if the preview is set at 500, then 500 samples will be recorded before the trigger point and 500 after.

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE	RANGE
#1	Z***:PREVIEW 1	500	1-999
#2	Z***:PREVIEW 2	500	1-999
#3	Z***:PREVIEW 3	500	1-999
#4	Z***:PREVIEW 4	500	1-999

## 5.5 ARMING

The channel must be armed before it can start recording data. Defined as a digital bit in the data table, it can be defined to arm on a high or low bit. The arming bit can be defined as the one bit allowing the logic analyzer to be turned on or off using only the keyboard. Default for all four recorders:

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:ARM BIT 1	D***:ONE BIT
#1	Z***:ARM LEVEL 1	Q***:HIGH
#2	Z***:ARM BIT 2	D***:ONE BIT
#2	Z***:ARM LEVEL 2	Q***:HIGH
#3	Z***:ARM BIT 3	D***:ONE BIT
#3	Z***:ARM LEVEL 3	Q***:HIGH
#4	Z***:ARM BIT 4	D***:ONE BIT
#4	Z***:ARM LEVEL 4	Q***:HIGH

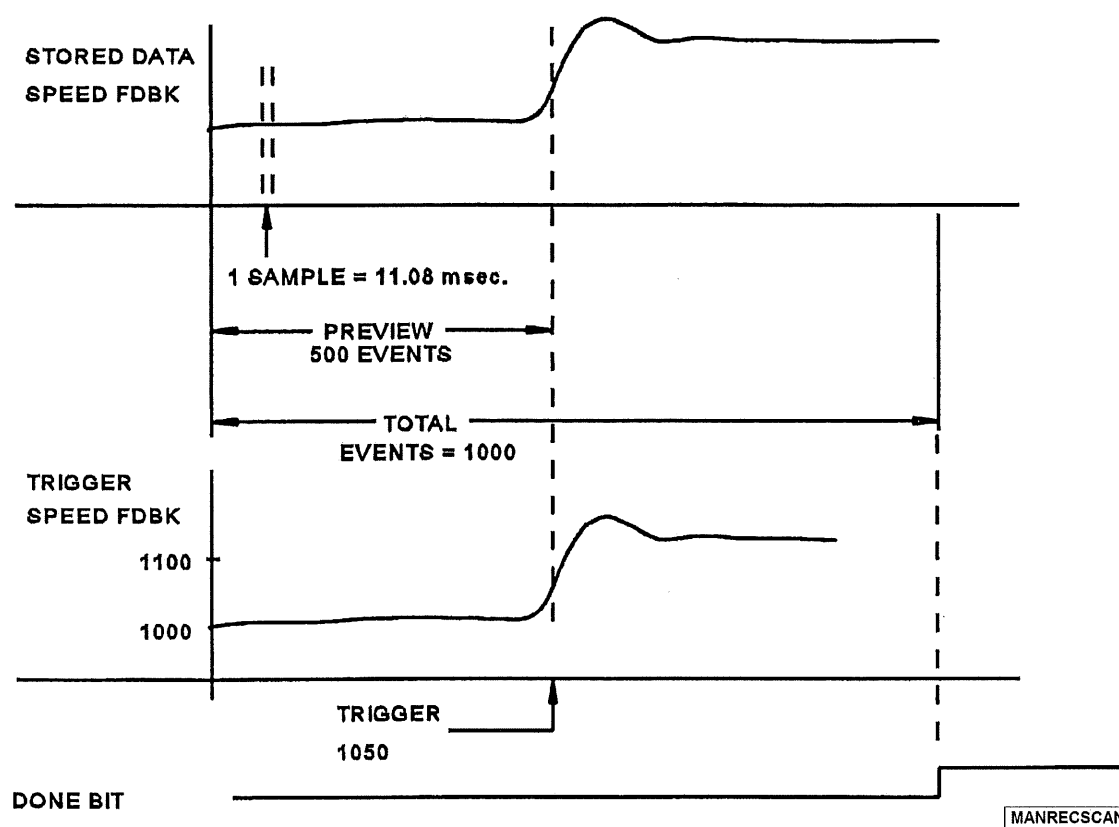


Figure 5-2. Manual Recording of Signal Analyzer

### Setup

Input Data:	ABS ACT SPD
Trigger:	Rising at 1,050 of ABS ACT SPD
Sample Rate:	1 = 11.11 ms
Total Time:	1,000 events X 11.11 ms = 11 seconds
Preview:	500 events
Output:	Zero bit
Reset:	Zero bit
Arm:	One bit
Enabled:	One bit

## Summary

The trigger is set to activate when ABS ACT SP exceeds 1,050. When triggered, data recording is completed. Upon completion, the channel is set to wait but is not reset. The data can be output manually (using the keyboard) or viewed. The channel may also be reset.

## 5.6 ENABLE

This bit enables or disables the recorder. The operator must disable the recorder for adjustments such as trigger level or sample rate. Defaults are as follows:

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:ENABLE REC1	Q***:DISABLED
#2	Z***:ENABLE REC2	Q***:DISABLED
#3	Z***:ENABLE REC3	Q***:DISABLED
#4	Z***:ENABLE REC4	Q***:DISABLED

## 5.7 RESET

Defined as a bit in the digital table which clears the done bit, it can be defined to reset on a high or low level. The recorder can also be reset by a keyboard bit. Default for all four recorders:

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:RESET BIT 1	D***:OUT DONE1
#1	Z***:RESET R/F 1	Q***:RISING
#2	Z***:RESET BIT 2	D***:OUT DONE2
#2	Z***:RESET R/F 2	Q***:RISING
#3	Z***:RESET BIT 3	D***:OUT DONE3
#3	Z***:RESET R/F 3	Q***:RISING
#4	Z***:RESET BIT 4	D***:OUT DONE4
#4	Z***:RESET R/F 4	Q***:RISING

## 5.8 DONE BIT

The done bit is high when the recorder has been armed, trigger activated, and the events stored. It stays high until the recorder has been disabled or reset. This bit can be used to relate to the human interface computer that recording is completed and data is ready to be uploaded.

RECORDER CHANNEL	CONFIGURATION PARAMETER
#1	D***:DONE REC1
#2	D***:DONE REC2
#3	D***:DONE REC3
#4	D***:DONE REC4

## 5.9 ANALOG OUT

The stored data can be output to an analog out. To do this the analog output must be configured to A\*\*\*:RECORDER. The output trigger bit can be configured to any digital data point. It can be enabled to output on a rising or falling edge.

The following sequence occurs when the data has been triggered to output:

The arming for the recorder is turned off. The oldest data point is scaled and outputted. It will then output one event every 27.7 ms. After the recording is outputted, the out done bit is set and rearms the recorder.

The out done bit is reset if the recorder is retriggered or if the analog out is selected again.

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#1	Z***:OUT TRIG 1	D***:ZERO BIT
	Z***:OUT R/F 1	Q***:RISING
	Z***:SPAN OUT 1	1.0
	Z***:OFF OUT 1	0.0
#2	Z***:OUT TRIG 2	D***:ZERO BIT
	Z***:OUT R/F 2	Q***:RISING
	Z***:SPAN OUT 2	1.0
	Z***:OFF OUT 2	0.0

RECORDER CHANNEL	CONFIGURATION PARAMETER	DEFAULT VALUE
#3	Z***:OUT TRIG 3	D***:ZERO BIT
	Z***:OUT R/F 3	Q***:RISING
	Z***:SPAN OUT 3	1.0
	Z***:OFF OUT 3	0.0
#4	Z***:OUT TRIG 4	D***:ZERO BIT
	Z***:OUT R/F 4	Q***:RISING
	Z***:SPAN OUT 4	1.0
	Z***:OFF OUT 4	0.0

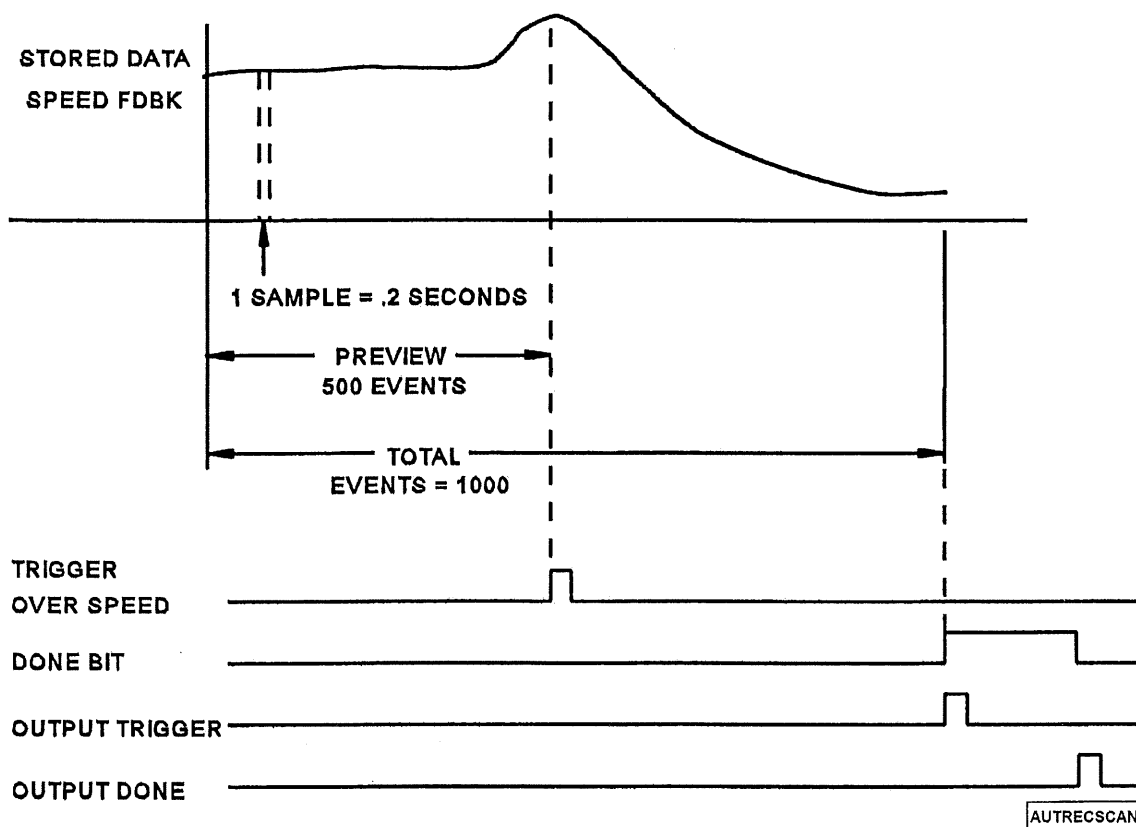


Figure 5-1. Automatic Recording of Signal Analyzer

Setup

Input Data:	ABS ACT SPD
Trigger:	Rising edge of Fault bit
Sample Rate:	18 (18 X 11.11 ms = .2 seconds/event)
Total Time:	1,000 events X .2 seconds = 200 seconds
Preview:	500 events
Output:	Rising edge of Done bit
Reset:	Rising edge of Output Done bit
Arm:	Run Enable
Enabled:	One bit

Summary

When triggered by an overspeed, speed feedback recording is completed by the recorder. The done bit is set upon collection of data, and the data is sent to either a computer or an analog output. The output done bit is set upon completion of the output, causing resetting of the channel. The channel is then ready to capture data on the next fault.





## **SECTION VI**

### **PREPARATION FOR USE**

Preparation for use of the ADDvantage-32 AC to DC Power Converter System includes unpacking, electrical interconnections, wiring instructions, and installation.

#### **6.1 UNPACKING**

Inspect all shipping containers for exterior damage. Notify the carrier of any damage detected so that the carrier representative may inspect the equipment and shipping containers.

When removing equipment from shipping containers, check carefully that loose items such as connectors, nomenclature plates, cables, manuals, etc., are removed before discarding packing materials. (Internal modules and connectors should be checked for proper seating.)

If the ADD-32 will not be installed right away, refer to Storage and Installation Specifications in Section 6.3 for storage instructions.

#### **6.2 MECHANICAL INSTALLATION AND SPECIFICATIONS**

Outline dimension drawings for the drive are found in the supplemental drawing manual and provide mounting dimensions for physical installation as well as electrical specifications, enclosure size specifications, grounding requirements, and wiring information. Recommendations for pulse generator coupling and timing devices are provided in the Avtron Rotary Pulse Generator Installation Instructions. Proper mounting of the pulse generator (speed feedback device) is critical for achieving optimum performance and reliability.

\*\*\*\*\*

**WARNING**

**WHEN CUTTING OR DRILLING INTO ANY ENCLOSURE HOUSING, ALWAYS MAKE SURE THAT METAL SHAVINGS DO NOT DROP ONTO THE COMPONENTS. AVTRON TAPES LARGE SHEETS OF PLASTIC TO THE PANEL AROUND THE COMPONENTS WHEN METAL SHAVINGS ARE LIKELY TO BE PRODUCED. WE RECOMMEND THE SAME TO INSTALLERS OF OUR EQUIPMENT.**

\*\*\*\*\*

TABLE 6-1. ADD-32 MECHANICAL SPECIFICATIONS

DRIVE PART NUMBER	WEIGHT	HEIGHT	WIDTH*	DEPTH
DC0010	55 lbs.	22.5"	12"	11.5"
DC0030	55 lbs.	22.5"	12"	11.5"
DC0056	55 lbs.	22.5"	12"	11.5"
DC0110	85 lbs.	28"	19"	12.25"
DC0180	130 lbs.	31"	16"	16.5"
DC0280	150 lbs.	34.5"	18"	17.75"
DC0360	150 lbs.	34.5"	18"	17.75"
DC0510	150 lbs.	34.5"	18"	17.75"
DC055X	250 lbs.	43.56"	21.12"	18.75"
DCXXXX FIELD CONTROLLER	35 lbs.	17.5"	12"	10.1"
DC054X ARMATURE BRIDGE	250 lbs.	33.3"	27.4"	17.66"
DC085X ARMATURE BRIDGE	250 lbs.	37.8"	27.4"	17.66"
DC155X-2 ARMATURE BRIDGE	400 lbs.	65.4"	24.1"	18.69"
DC155X-4 ARMATURE BRIDGE	600 lbs.	65.4"	24.1"	18.69"
DC155X-A ARMATURE BRIDGE	575 lbs.	66.5"	26.0"	19.50"
DC155X-B ARMATURE BRIDGE	750 lbs.	66.5"	26.0"	19.50"
DC250X ARMATURE BRIDGE	1,400 lbs.	67.1"	38.7"	23.00"
DC300X-A ARMATURE BRIDGE	1,050 lbs.	67.1"	38.7"	23.00"
DC300X-B ARMATURE BRIDGE	1,400 lbs.	67.1"	38.7"	23.00"

\*Not including AC input power bus bars.

### **6.3 STORAGE AND INSTALLATION SPECIFICATIONS**

If the ADD-32 is to be stored for an extended period of time prior to its installation, the storage temperature should not fall below -20°C and noncondensing humidity should be no more than 95%. Installation conditions require an ambient temperature of 0-40°C when enclosed. Refer to the outline drawing provided in the drawing package for enclosure size and cooling specifications. No derating is needed at altitudes between 0-3,300 feet above sea level.

### **6.4 MOUNTING SPECIFICATIONS**

All ADDvantage-32 models should be mounted vertically against a flat panel to allow necessary cooling.

### **6.5 LOCATION**

The equipment should be located where the operating ambient temperature does not exceed 50°C within an enclosure and where excessive shock and vibration are not transmitted to the units. The equipment should be isolated from or protected against such adverse environmental conditions as oil or water spray, and corrosive or conductive air contaminants. Ideally, the equipment should be installed in an air-conditioned control room. Refer to appropriate outline drawing for specific enclosure and ambient temperature restrictions.

#### Location of Other Equipment

The ADD-32 Power Converter should be installed with sufficient distance from other equipment so that the door may be opened during installation, maintenance, and servicing without interfering with other equipment.

## 6.6

**ELECTRICAL CONNECTIONS**

\*\*\*\*\*

**WARNING**

DO NOT OPERATE RADIO TRANSMITTERS or CELL PHONES IN THE VICINITY OF THE ADD-32. The ADD-32 is an electronic device. Although it is designed to operate reliably in typical industrial environments, the ADD-32 can be affected by radio and/or cell phone transmitters. It is possible to cause drive faults, inappropriate/unintended drive I/O activity, and unpredictable operation that could result in damage to the ADD-32, damage to other equipment, or serious injury to personnel.

Radio transmitter interference is a site specific phenomena. Generally, electrical wires connected to terminals on the ADD-32 are the conduits for radio interference. Interference can be minimized by good wiring design and installation practice. It is recommended that signs be posted in and around the drive system, warning of the possibility of interference if the drive is in operation. DO NOT USE radio transmitters or cell phones in the area.

Absence of a radio interference problem is no guarantee that a problem will never occur as conditions and environments can change.

\*\*\*\*\*

The following information is for assistance in wiring the ADDvantage-32 in accordance with specifications set forth by the National Electrical Code. Always review local building and electrical codes before making electrical connections to this device. Refer to the appropriate outline drawing and rating nameplate for power requirements, fault current interrupt rating, control power output rating, and field output and armature output ratings. Wire units using copper wire with a minimum of 75°C insulation.

## 6.6.1

**510 ADC AND BELOW**

Wire termination kits which provide necessary wire termination lugs for connection of units rated at 510 ADC and below in accordance with the National Electrical Code and Underwriters Laboratory are available. See Tables 6-2 and 6-2a to identify the part number of the appropriate kit. The instructions included with these kits detail the correct wire gauge used at each connection point and proper torque requirements.

TABLE 6-2. WIRE TERMINATION KIT GUIDE FOR PART NUMBERS  
WITHOUT "N" IN THE NINTH POSITION  
(Example: DC0056-4D02-C)

↑

DRIVE PART NO.	WIRE TERMINA- TION KIT PART NO.	AC INPUT (L1,L2,L3)		MOTOR ARMATURE OUTPUT (A1,A2,DB)		CHASSIS GROUND		MOTOR FIELD***
		Stud Size	Recommended Wire Size	Bolt Size	Recommended Wire Size	Bolt Size	Recommended Wire Size	
DC0010	A20741	1/4"	10 AWG	*	10 AWG	1/4-20	10 AWG	12 AWG
DC0030	A20742	1/4"	10 AWG	*	8 AWG	1/4-20	10 AWG	12 AWG
DC0056	A20743	1/4"	6 AWG	*	4 AWG	1/4-20	10 AWG	12 AWG
DC0110	A20744	1/4"	1/0 AWG	*	2/0 AWG	1/4-20	6 AWG	12 AWG
DC0180	A20745	3/8"	3/0 AWG	1/4-20	2 × 1/0 AWG **	3/8-16	6 AWG	12 AWG
DC0280	A20746	3/8"	2 × 1/0 AWG **	3/8-16	500 MCM	3/8-16	4 AWG	12 AWG
DC0360	A20747	3/8"	2 × 3/0 AWG **	3/8-16	2 × 4/0 AWG **	3/8-16	2 AWG	12 AWG
DC0510	A20748	3/8"	2 × 300 MCM **	1/2" STUD	2 × 400 MCM **	3/8-16	1/0 AWG	12 AWG

\* Wire termination is made to lug attached to the drive contactor (K1).

\*\* Indicates two wires of the same size in parallel.

\*\*\* No lugs are required for these connections. Strip insulation 0.31" from end of wire. Make connections to TB1 on top of the drive.

TABLE 6-2A. WIRE TERMINATION KIT GUIDE FOR PART NUMBERS  
WITH "N" IN THE NINTH POSITION  
(Example: DC0056-4DN2-C)



DRIVE PART NO.	WIRE TERMINA- TION KIT PART NO.	AC INPUT (L1,L2,L3)		MOTOR ARMATURE OUTPUT (A1,A2,DB)		CHASSIS GROUND		MOTOR FIELD***
		Stud Size	Recommended Wire Size	Bolt Size	Recommended Wire Size	Bolt Size	Recommended Wire Size	Recommended Wire Size
DC0010	A21560	1/4"	10 AWG	***	10 AWG	1/4-20	10 AWG	12 AWG
DC0030	A21561	1/4"	8 AWG	***	6 AWG	1/4-20	10 AWG	12 AWG
DC0056	A21562	1/4"	4 AWG	*	2 AWG	1/4-20	10 AWG	12 AWG
DC0110	A21563	1/4"	1/0 AWG	1/4" STUD	2/0 AWG	1/4-20	6 AWG	12 AWG
DC0180	A21564	3/8"	4/0 AWG	3/8" STUD	2 × 1/0 AWG **	3/8-16	6 AWG	12 AWG
DC0280	A21565	3/8"	2 × 2/0 AWG **	3/8" STUD	2 × 3/0 AWG **	3/8-16	4 AWG	12 AWG
DC0360	A21566	3/8"	2 × 3/0 AWG **	3/8" STUD	2 × 250 MCM **	3/8-16	2 AWG	12 AWG
DC0510	A21567	3/8"	2 × 300 MCM **	1/2" STUD	2 × 400 MCM **	3/8-16	1/0 AWG	12 AWG

\* Wire termination is made to lug attached to the drive contactor (K1).

\*\* Indicates two wires of the same size in parallel.

\*\*\* No lugs are required for these connections. Strip insulation 0.31" from end of wire. Make connections to TB1 on top of the drive.

### NOTE

Refer to rating nameplate for voltage and current ratings. Recommended wire sizes are based on NEC TABLES 310-16 and 310-17 for copper wire. Conductor sizes are based on 60°C table for currents below 100A and 75°C table for currents above 100A. Derating factor of 0.82 for 60 degree wire used in 36-40 degree ambient, 0.88 for 75 degree wire used in 36-40 degree ambient. See N.E.C. Section 250-95 for grounding conductor sizing. Sizes may also be adjusted to meet certain lug compatibility/requirements. These sizes may differ from the drive internal and panel wires. Always consult local building codes to determine the requirements of your application.

The 3-phase AC input power connections (L1, L2, L3) are made to studs on top of the drive base assembly. (Refer to Table 6-2 or 6-2a.) These connections require terminal lugs for proper connection.

Motor armature (A1, A2) and dynamic braking (DB) connections are made to terminals attached to the output contactor at the top of the drive. Drive sizes DC0010, DC0030, and DC0056 provide lugs at these points. Drive sizes DC0110, DC0180, DC0280, DC0360, and DC0510 provide bolts but require terminal lugs for proper connections. Refer to Table 6-2 or appropriate outline drawing to determine correct wire terminations.

Motor field output connections are made to terminals 1 and 2 of terminal block TB1 located on top of the drive base assembly. No terminal lugs are required. Use #22 AWG to #8 AWG wire. Strip insulation 0.59" from end of wire.

### **NOTE**

Refer to appropriate outline drawing to determine voltage and current ratings.

Optional auxiliary field excitation transformer connections are made directly to TB1 terminals 3, 4, 5 and 6. Use #22 AWG to #12 AWG wire. Strip insulation 0.39" from end of wire.

Auxiliary control power connections are made directly to TB1 terminals 7 and 8. Use #22 AWG to #12 AWG wire. Strip insulation 0.47" from end of wire.

M-Contactor auxiliary contact connections are made to TB1 terminals 14, 15, and 16. These are rated to interrupt at a maximum of 5A, 300 V. Use #22 AWG to #14 AWG wire. Strip insulation 0.39" from end of wire.

Additional control connections such as E-STOP, E-STOP RESET, and DOK OUT are made to the quick connect plug connector at TB1 terminals 11, 12, 13, and 17, 18, 19, and 20. Use #22 AWG to #14 AWG wire. Strip insulation 0.27" from end of wire.

System interconnections such as digital and analog inputs and outputs, tach, serial link, etc., are made to the quick connect terminal blocks on the left side of the drive. No lugs are required for these connections. Use #22 AWG to #14 AWG wire. Strip insulation 0.27" from the end of the wire.

For control power transformer configuration, see paragraph 6.6.4.

## 6.6.2

550 ADC

The 3-phase AC input power connections (L1, L2, L3) and the motor armature connections (A1, A2) are made to terminals on top of the drive base assembly. These connections require terminal lugs for proper connection. Drive size DC0550 has lugs attached for each of the connection points. Refer to Table 6-3 for recommended wire sizes.

Motor field output connections are made to terminals + and - of terminal block TB1 located at the bottom of the drive base assembly. No terminal lugs are required. Use #12 AWG to #4 AWG wire. Strip insulation 0.59" from end of wire.

**NOTE**

Refer to appropriate outline drawing to determine voltage and current ratings.

Optional auxiliary field excitation transformer connections are made directly to TB1 terminals 3, 4, 5 and 6. Use #12 AWG to #4 AWG wire. Strip insulation 0.39" from end of wire.

Auxiliary control power connections are made directly to TB1 terminals 7 and 8. Use #22 AWG to #12 AWG wire. Strip insulation 0.47" from end of wire.

M-Contactor auxiliary contact connections are made to TB1 terminals 14, 15, and 16. These are rated to interrupt at a maximum of 5A, 300 V. Use #22 AWG to #14 AWG wire. Strip insulation 0.39" from end of wire.

Additional control connections such as E-STOP, E-STOP RESET, and DOK OUT are made to the quick connect plug connector at TB1 terminals 11, 12, 13, and 17, 18, 19, and 20. Use #22 AWG to #14 AWG wire. Strip insulation 0.27" from end of wire.

System interconnections such as digital and analog inputs and outputs, tach, serial link, etc., are made to the quick connect type terminal blocks on the left side of the drive. No lugs are required for these connections. Use #22 AWG to #14 AWG wire. Strip insulation 0.27" from the end of the wire.

For control power transformer configuration, see paragraph 6.6.4.



TABLE 6-3. RECOMMENDED WIRE SIZES

DRIVE PART NO.	AC INPUT (L1,L2,L3)	FIELD SUPPLY (L1,L2)	MOTOR ARMATURE (A1,A2)	MOTOR FIELD (+,-)	CHASSIS GROUND (ARMATURE BRIDGE)		CHASSIS GROUND (FIELD SUPPLY)	
	Recommended Wire Size*	Recommended Wire Size**	Recommended Wire Size*	Recommended Wire Size**	Bolt Size***	Recommended Wire Size	Bolt Size	Recommended Wire Size
DC0540	2 × 300 MCM	10 AWG	2 × 500 MCM	12 AWG	3/8-16	1/0 AWG	1/4-20	14 AWG
DC0541	2 × 300 MCM	8 AWG	2 × 500 MCM	10 AWG	3/8-16	1/0 AWG	1/4-20	10 AWG
DC0542	2 × 300 MCM	6 AWG	2 × 500 MCM	6 AWG	3/8-16	1/0 AWG	1/4-20	10 AWG
DC0550	2 × 350 MCM	N. A.	2 × 500 MCM	14 AWG	One ground connection. No lugs required.	1/0 AWG	N. A.	N. A.
DC0551	2 × 350 MCM	N. A.	2 × 500 MCM	10 AWG		1/0 AWG	N. A.	N. A.
DC0552	2 × 350 MCM	N. A.	2 × 500 MCM	10 AWG		1/0 AWG	N. A.	N. A.
DC0850	3 × 350 MCM	10 AWG	3 × 500 MCM	12 AWG	3/8-16	2/0 AWG	1/4-20	14 AWG
DC0851	3 × 350 MCM	8 AWG	3 × 500 MCM	10 AWG	3/8-16	2/0 AWG	1/4-20	10 AWG
DC0852	3 × 350 MCM	6 AWG	3 × 500 MCM	6 AWG	3/8-16	2/0 AWG	1/4-20	10 AWG
DC1550	5 × 500 MCM	10 AWG	6 × 500 MCM	12 AWG	3/8-16	4/0 AWG	1/4-20	14 AWG
DC1551	5 × 500 MCM	8 AWG	6 × 500 MCM	10 AWG	3/8-16	4/0 AWG	1/4-20	10 AWG
DC1552	5 × 500 MCM	6 AWG	6 × 500 MCM	6 AWG	3/8-16	4/0 AWG	1/4-20	10 AWG
DC3000	**** 6 × 1250 MCM or 8 × 700 MCM	10 AWG	**** 8 × 1000 MCM	12 AWG	1/2-13 × 1.25	400 MCM	1/4-20	14 AWG
DC3001	**** 6 × 1250 MCM or 8 × 700 MCM	8 AWG	**** 8 × 1000 MCM	10 AWG	1/2-13 × 1.25	400 MCM	1/4-20	10 AWG
DC3002	**** 6 × 1250 MCM or 8 × 700 MCM	6 AWG	**** 8 × 1000 MCM	6 AWG	1/2-13 × 1.25	400 MCM	1/4-20	10 AWG

\* Multiple conductors run in parallel. Lugs are supplied attached to input and output bus bars.

\*\* No lugs are required for these connections. Make connections to TB1 on top of the field supply assembly. Strip insulation 0.59" from end of wire.

\*\*\* Ground lugs are provided attached to these bolts on both sides of the chassis. See outline drawings for wire size range of these lugs.

\*\*\*\* These units are designed for direct bus bar connection. However, the multiple wire connections indicated may be used.

### 6.6.3 540, 850, 1550, and 3000 ADC

Use the following information to wire units rated at 540, 850, 1550, and 3000 ADC in accordance with the National Electrical Code. Always review local building and electrical codes before making electrical connections to this device. Refer to Table 6-3 for recommended wire sizes.

System interconnections such as digital and analog inputs and outputs, tach, serial link, etc., are made to the quick connect type terminal blocks on the left side of the drive. No lugs are required for these connections. These terminals accept #22 to #16 AWG wire. Strip insulation 0.27" from the end of the wire.

Auxiliary field excitation transformer, emergency stop, E-stop reset, M-contactor coil and aux contacts, armature bridge blower, and aux control power transformer connections are made to the rail-mounted terminal block (TB1) on top of the field supply and (TB2) on the bottom. No lugs are required for these connections. These terminals accept #22 to #14 AWG wire. Strip insulation 0.39" from the end of the wire.

### 6.6.4 CONTROL POWER TRANSFORMER CONFIGURATION

#### 10-510 ADC Drives

The control transformer (T1) is located near the bottom of the base assembly. Refer to Figure 6-1. Set the jumpers on T1 for the correct incoming AC line voltage (230 or 460 VAC).

#### 550 ADC Drive

The control transformer (T1) is located near the right-center of the base assembly. This model may be configured for 230, 460, or 575 VAC input. Transformer terminals H2, H3, and H4 are used to set the transformer's input voltage. Refer to Figure 6-3 (Block Diagram, Power Connections, 550 ADC) or the drive schematic D26053 for configuration connection points. If the unit is to be operated at 230 VAC, remove the input wire from terminal H3 and connect it to terminal H2. For 575 VAC, remove the input wire from terminal H3 and connect it to terminal H4. See step 7 of paragraph 7.7 for required fuse change information.

#### 540, 850, 1550 and 3000 ADC Drives

The control transformer is mounted external to the drive.

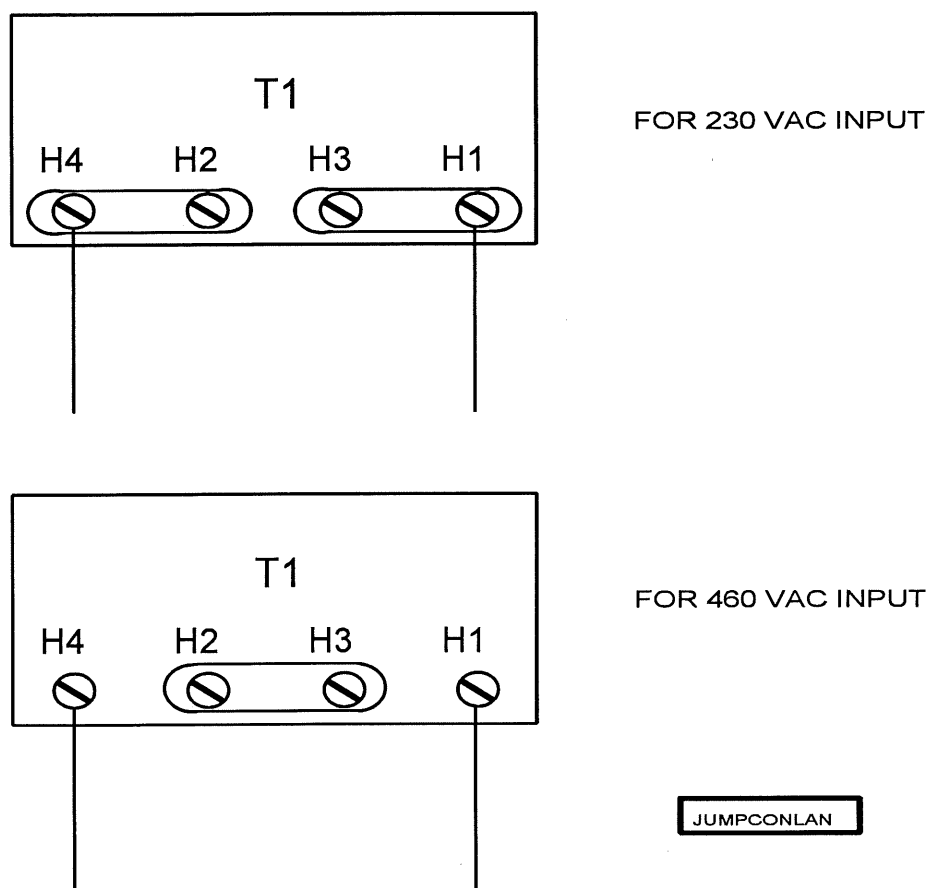


Figure 6-1. T1 Jumper Configuration (10-510 ADC Drives)

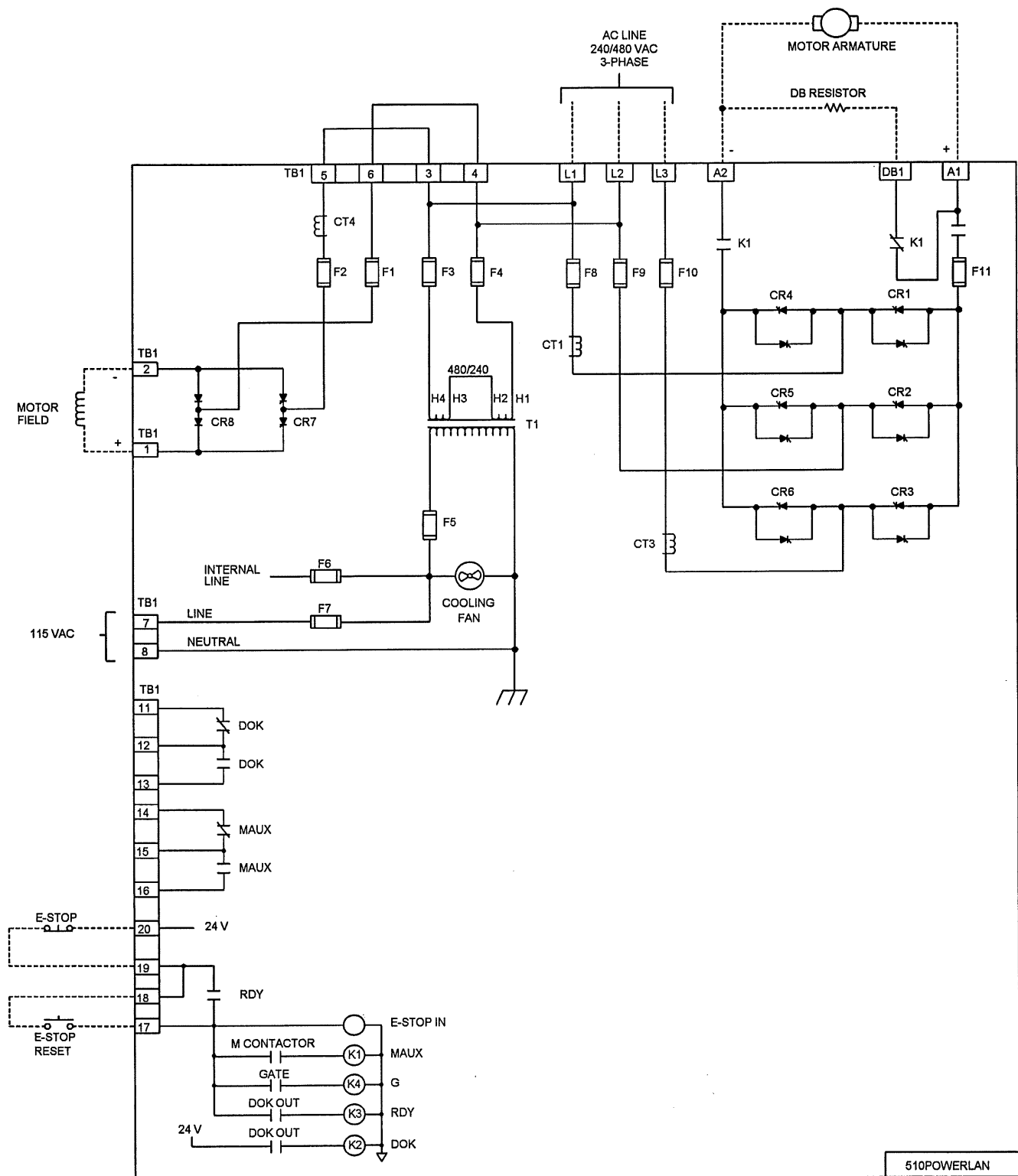


Figure 6-2A. Block Diagram, Power Connections, 510 ADC and Below  
Exception: See Figure 6-2B for 110A Drives Model DC0110-4 □ L0-C.

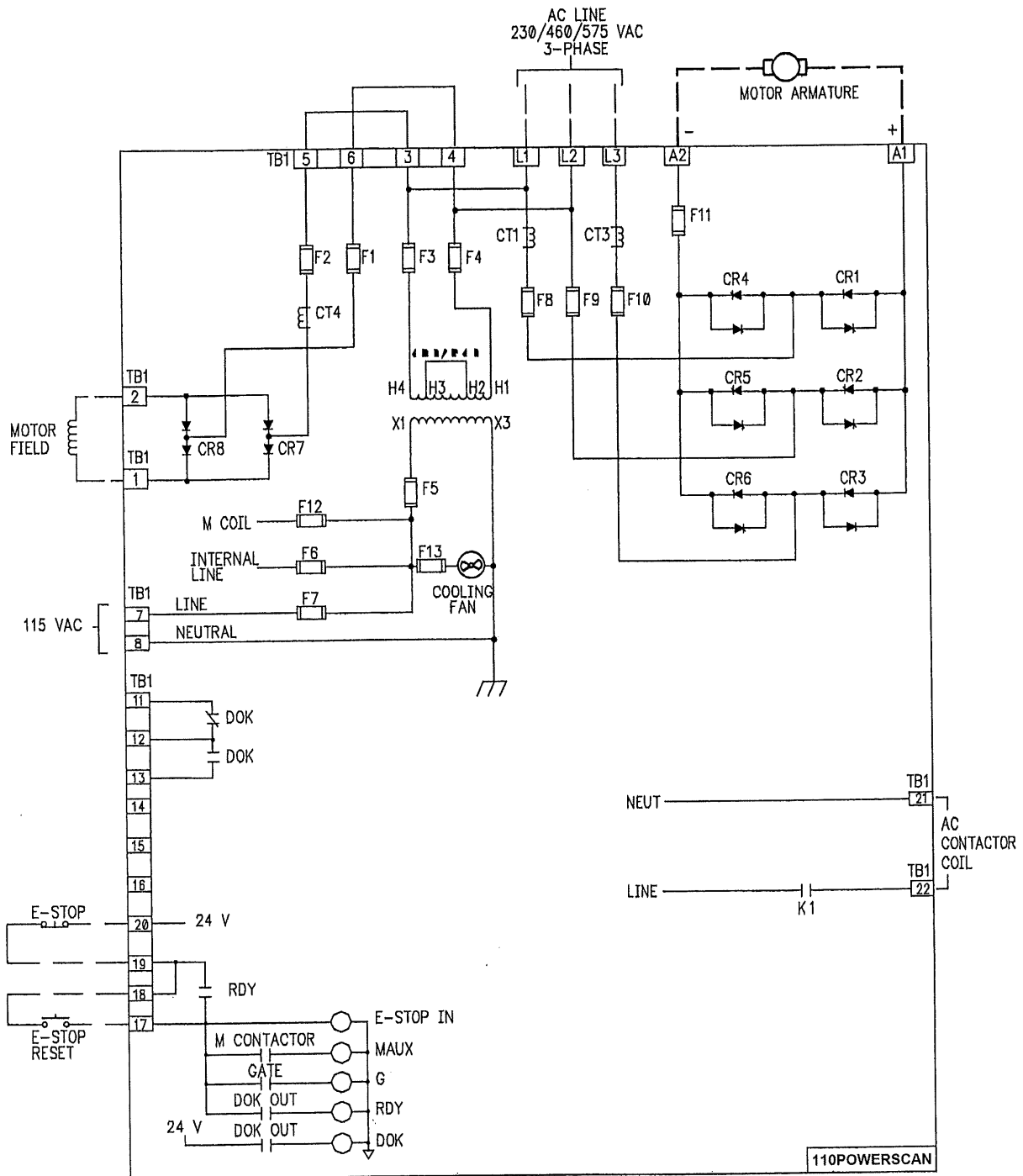


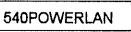
Figure 6-2B. Block Diagram, Power Connections, 110 ADC

Used Only on DC0110-4 □ L0-C

(External DC Contactor)



6-14



### NOTE

DC155X-A&B and DC300X units have parallel fuse assemblies in the F1 through F6 positions.

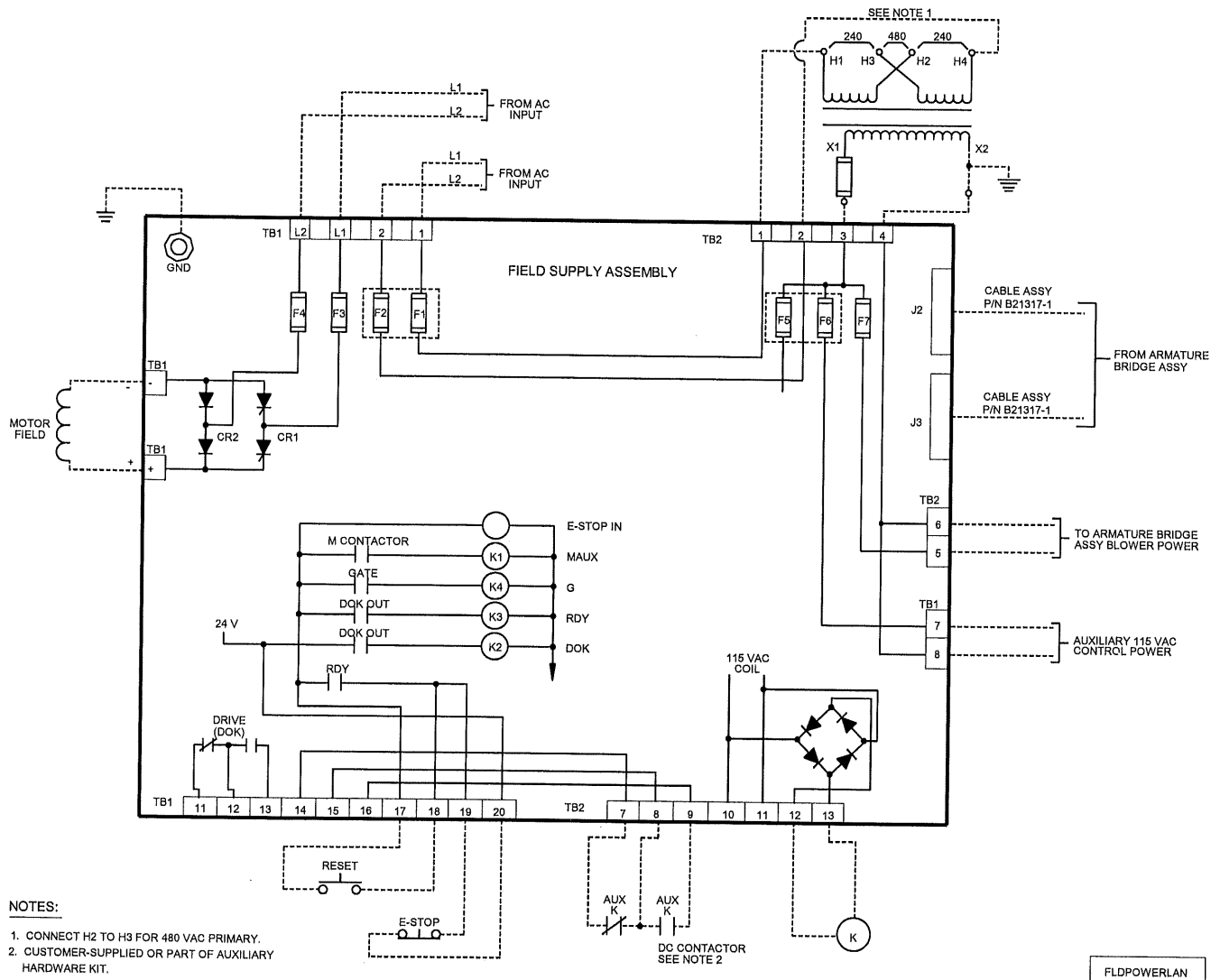


Figure 6-5. Block Diagram, Field Supply Assembly  
Power Connections (540, 850, 1550, 3000 ADC)



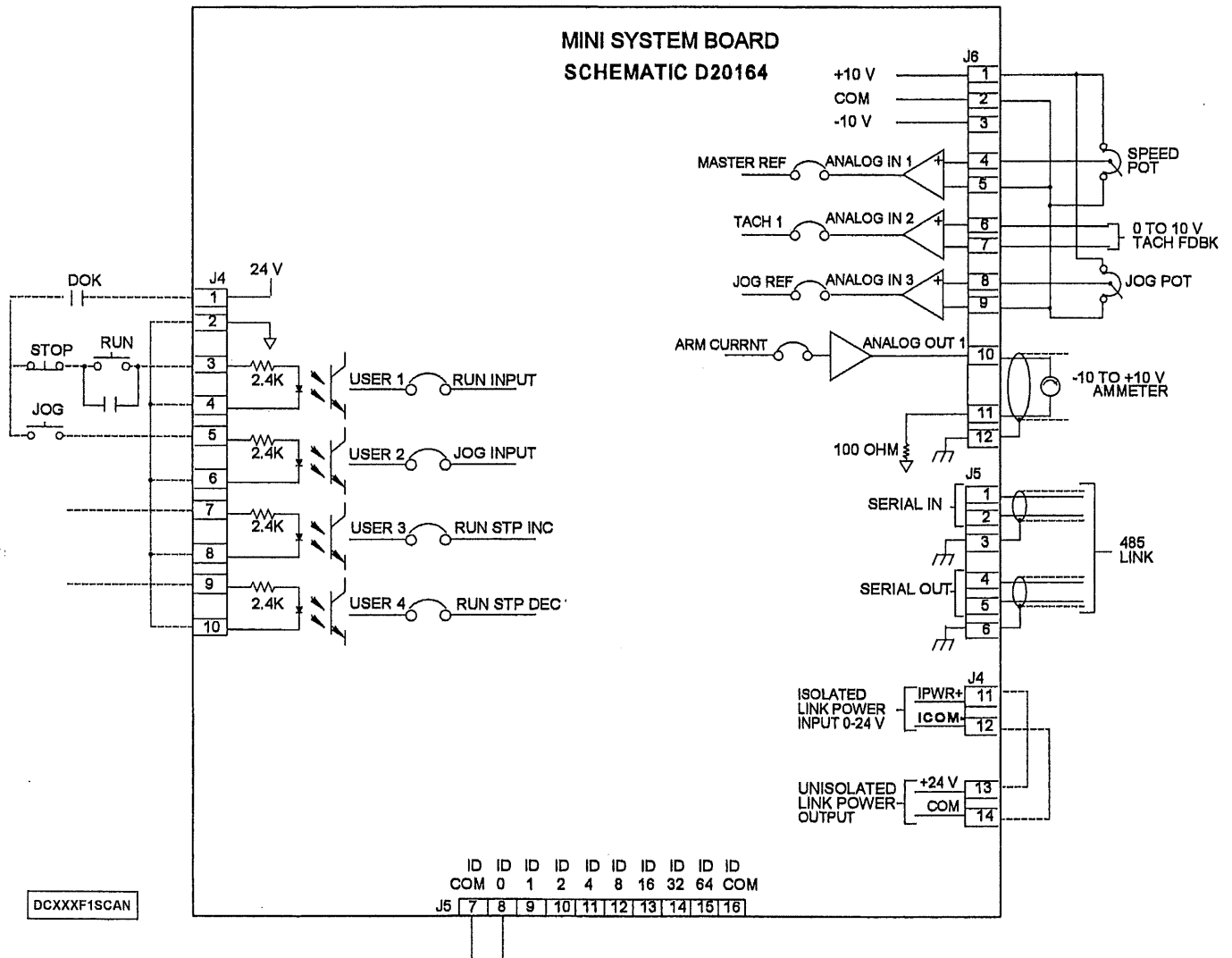


Figure 6-6. Block Diagram, Mini System Board

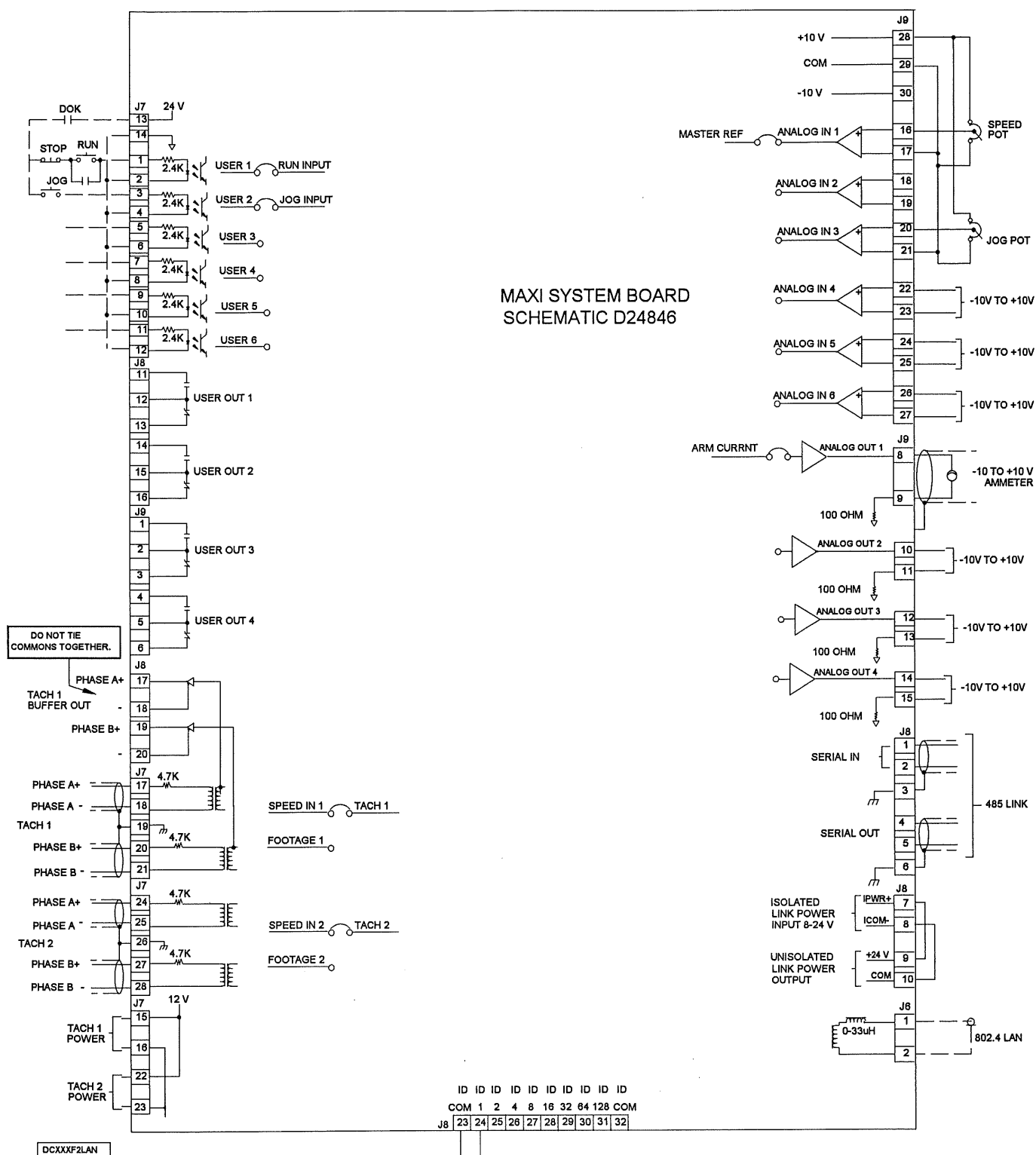


Figure 6-7. Block Diagram, Maxi System Board

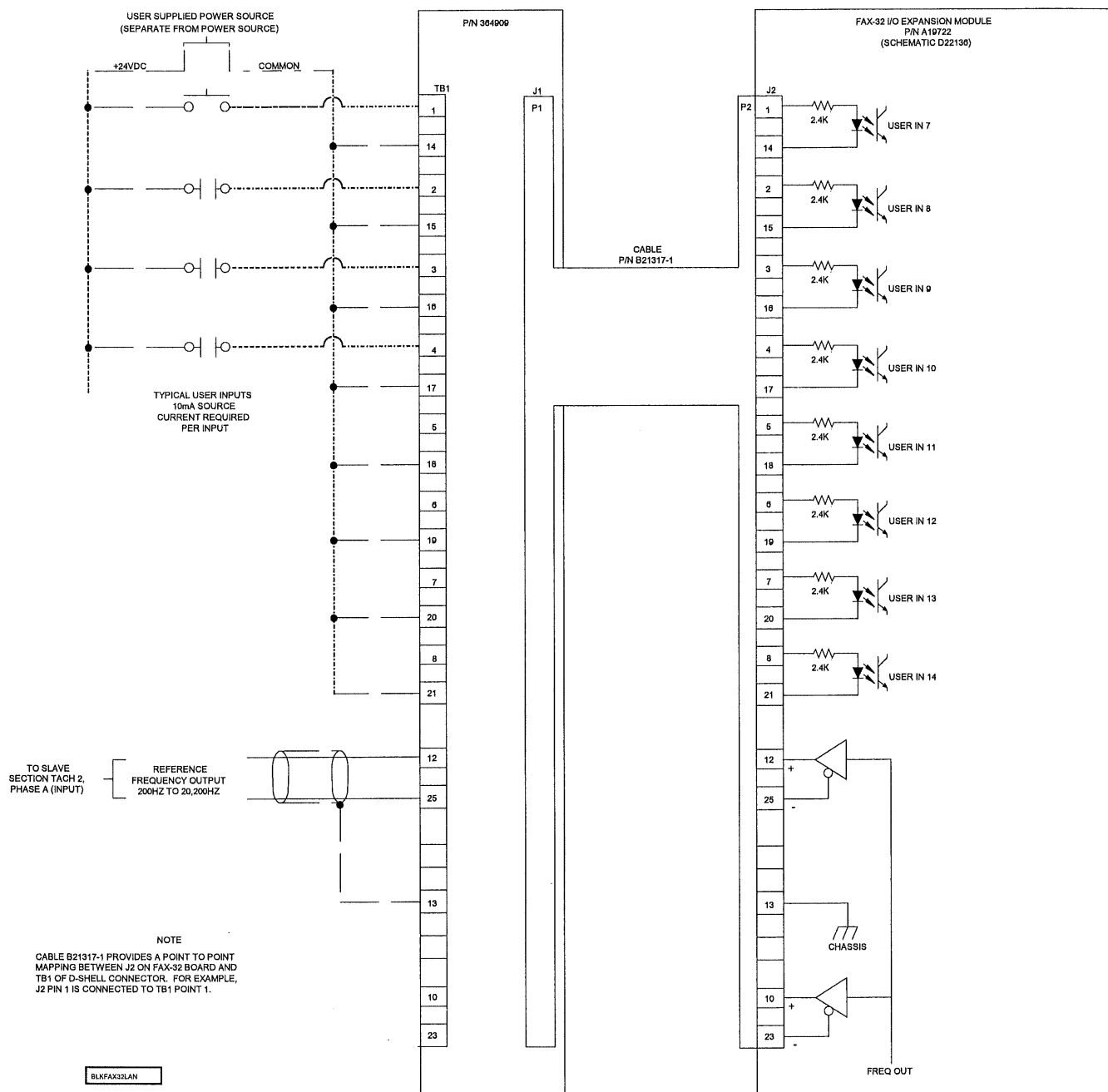


Figure 6-8. Block Diagram, FAX-32 Board

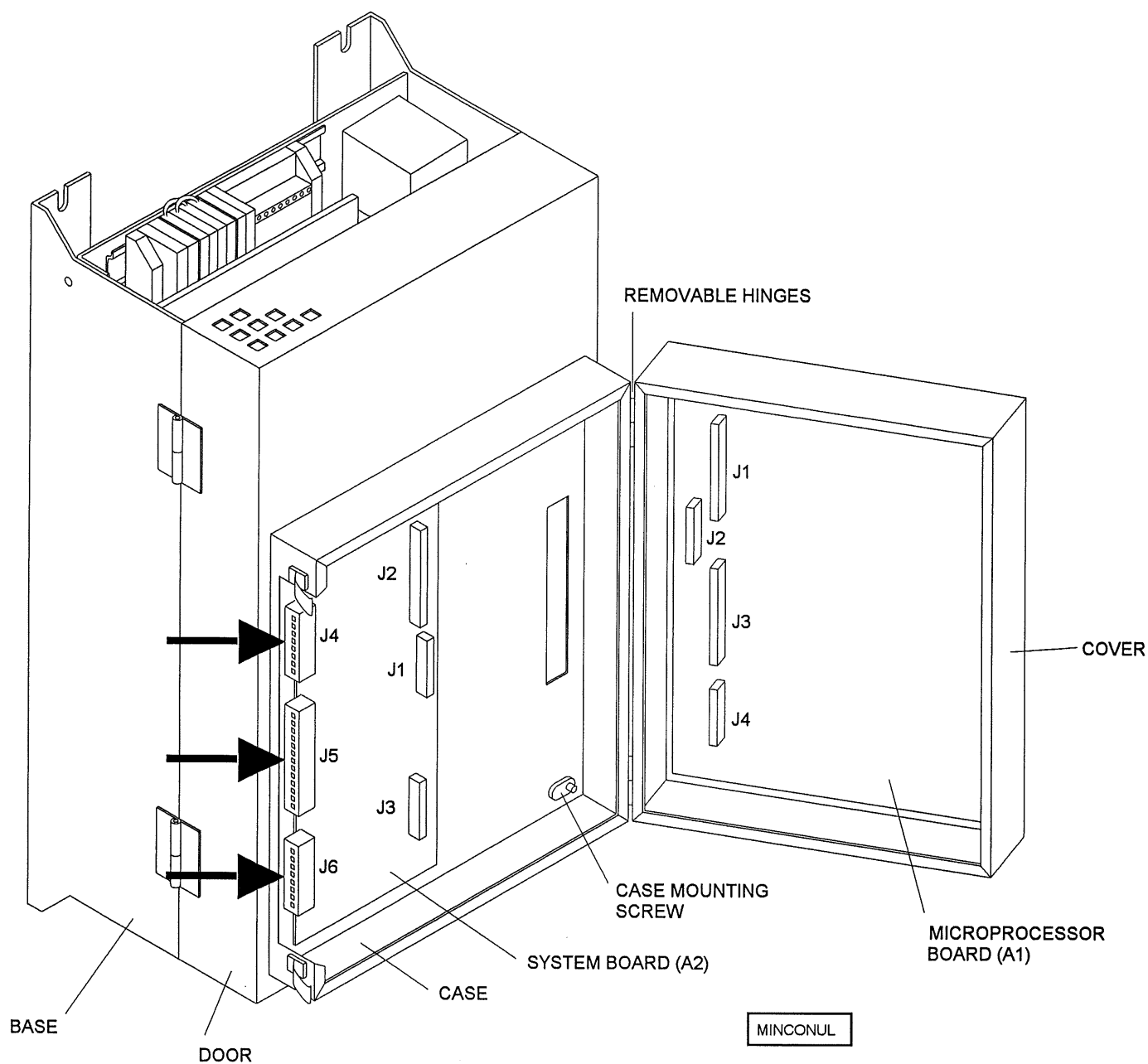


Figure 6-9. Mini System Board Interconnections

**NOTE**

Board interconnections are the same for all ADD-32 units.

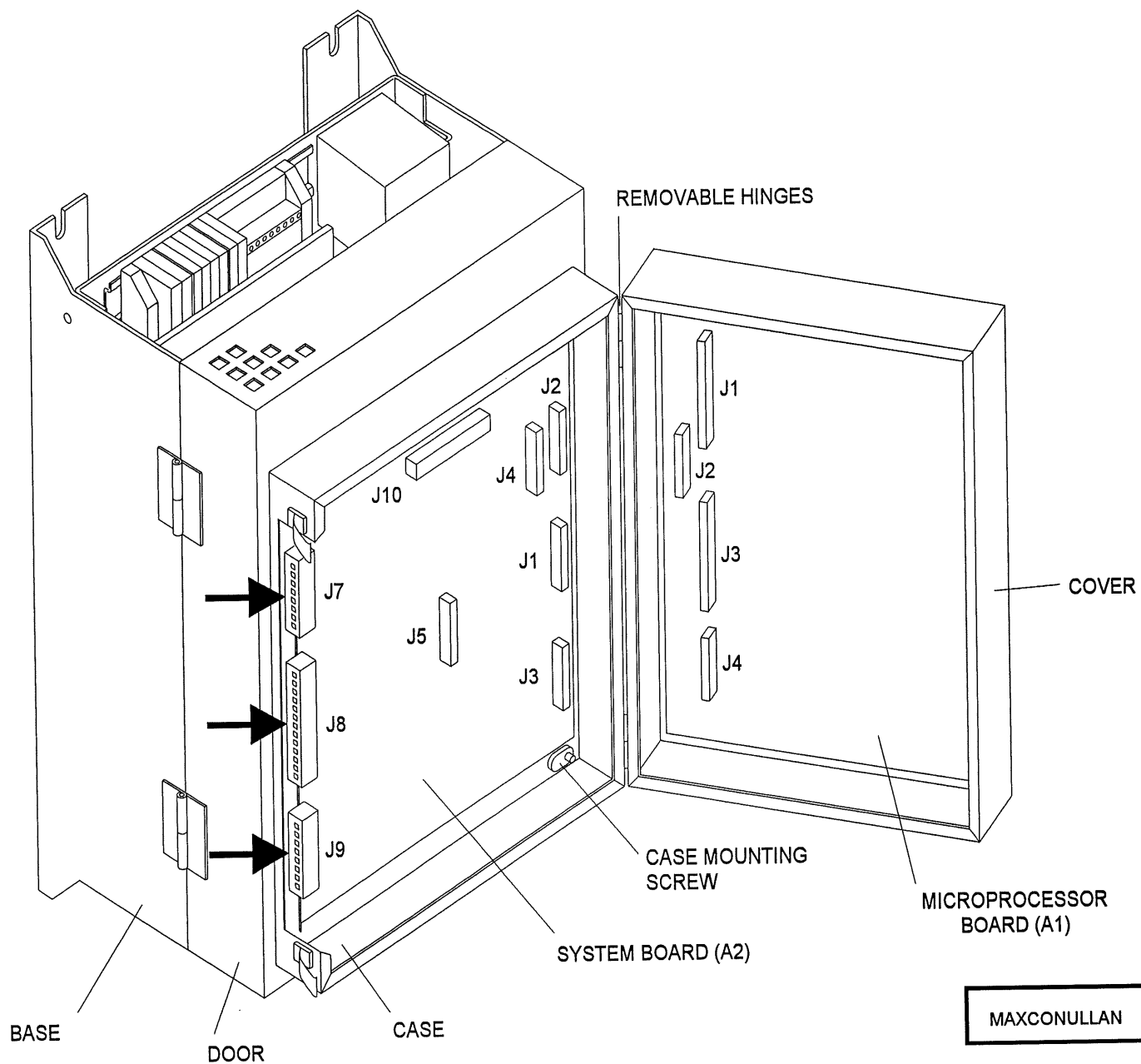


Figure 6-10. Maxi System Board Interconnections

**NOTE**

Board interconnections are the same for all ADD-32 units.

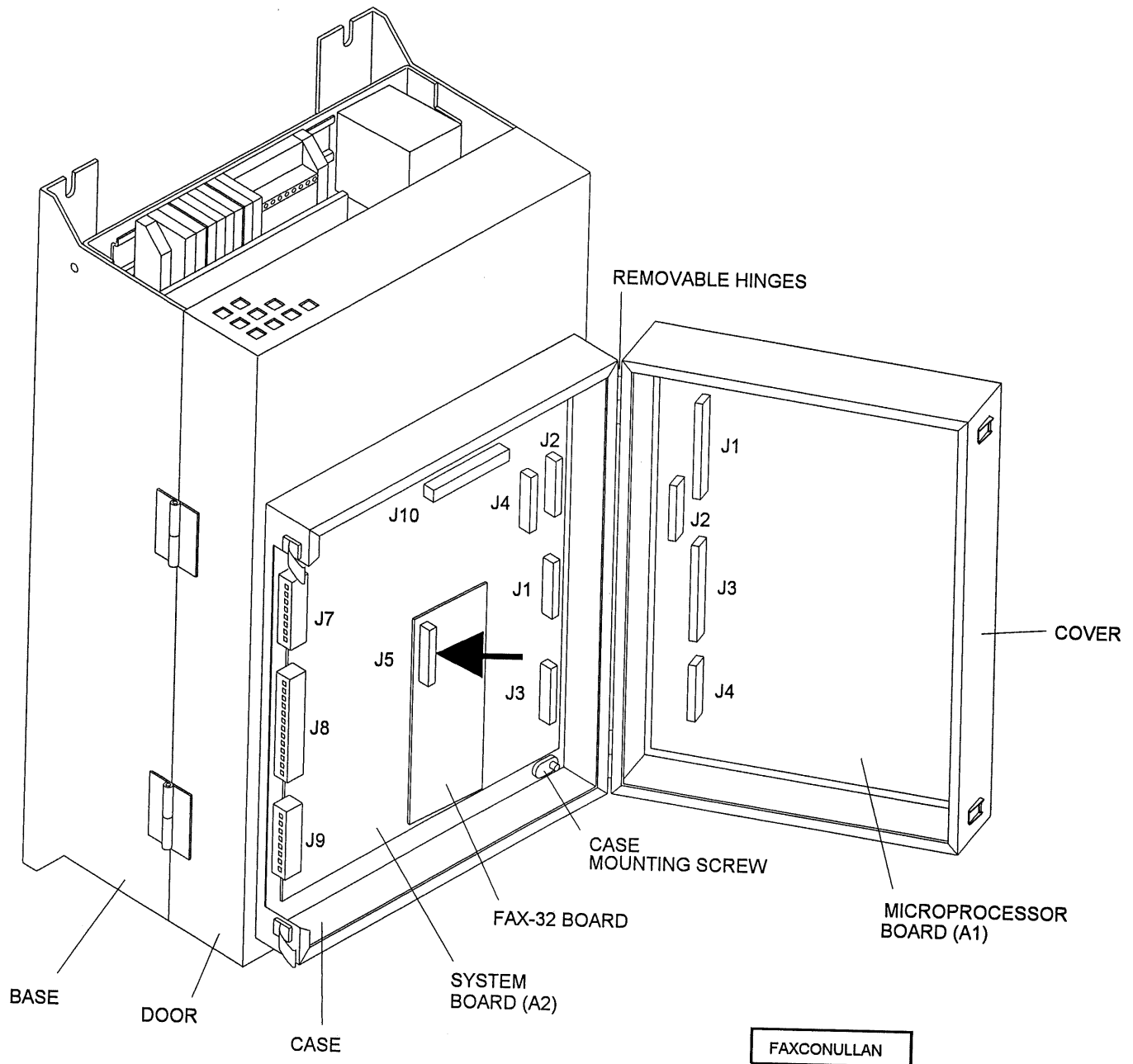


Figure 6-11. FAX-32 Board Interconnections

**NOTE**

Board interconnections are the same for all ADD-32 units.

## 6.7 ELECTRICAL INSTALLATION

Interconnection wiring and connection diagrams are provided in the supplemental drawing manual and are identified in that Table of Contents. These drawings include part numbers of the major assemblies, and corresponding Schematic/Interconnection Wiring Diagrams.

### WIRING PRACTICES AND NOTES

\*\*\*\*\*

#### **W A R N I N G**

**THIS EQUIPMENT CONTAINS HAZARDOUS VOLTAGES. THE MAIN DISCONNECT DEVICE MAY NOT REMOVE ALL HAZARDOUS VOLTAGE SOURCES. TO AVOID LOSS OF LIFE, SEVERE PERSONAL INJURY, OR PROPERTY DAMAGE, FOLLOW ALL INSTRUCTIONS CONTAINED IN THIS MANUAL AS WELL AS PROPER SAFETY PRACTICES.**

**HAZARDOUS VOLTAGES MAY ALSO BE PRESENT ON EXTERNAL SURFACES OF THE CONTROLLER CASE, IF NOT PROPERLY GROUNDED. AVOID LOSS OF LIFE, SEVERE PERSONAL INJURY, OR SUBSTANTIAL PROPERTY DAMAGE BY FOLLOWING SAFETY PRACTICES.**

\*\*\*\*\*

#### **NOTE**

All conductor sizes referenced in this manual are for copper conductors with a minimum insulation rating of 75°C.

Before wiring units according to the Interconnection Diagrams, review the following notes applying to routing and termination of interconnection cables.

It is recommended that power cables and signal cables be routed in separate conduit. When using cable trays, route power lines in different trays and keep parallel power trays at a maximum distance from signal wires to avoid possible "cross-talk".

All pulse generator cables may be run in common conduit or cable trays because these cables include an electromagnetic shield.

Use of conduit is generally recommended instead of cable trays because protection against physical or chemical damage is provided and, if grounded, electromagnetic shielding is provided.

Use the following guidelines to simplify wiring of the individual cables to respective terminal boards in the drive and to minimize the possibility of electrical noise ("cross-talk") between conductors in different cables.

1. Avoid excessive lengths of cable or individual conductors.
2. While preparing each cable for connection to the terminal strip, cut back and remove the cable covering so that exposed insulated wires extend the length of the terminal strip.
3. Locate the terminal connection point for each wire. Trim the wire to length, allowing just enough slack to avoid the wiring being pulled taut over terminal strips or their wiring after harnessing. All terminals should be accessible. Strip back the insulator approximately 3/8" on each conductor.
4. Printed circuit board mounted terminal blocks have clamping type terminals for interconnection of cables. Therefore, it is not necessary to tin and add lugs to the wires before connection to the terminal board. The stripped wire ends are inserted under a clamping plate, and a screw tightens the plate down over the wires, securing the connection.

#### **NOTE**

Use caution in stripping the insulation from wires and tightening terminals of terminal blocks. Incorrect stripping or tightening may result in damage to equipment and or injury to personnel.

#### **NOTE**

Do not bundle signal and power cables/wires in a common harness. Separate power wires from signal wires as much as possible.



## **6.8           INSTALLATION CHECKOUT**

After all equipment is mounted and wired, check over the entire installation to be sure that all mounting hardware is secure, all pulse generators are properly aligned, and all wiring interconnections are in accordance with the diagrams in this manual.

### **NOTE**

Insure that ground cables are properly attached to the drive chassis. Refer to the outline drawing (in drawing package) for location of grounding points. Note that the 540 amp and above drives have grounding lugs attached to both the armature bridge chassis and the field supply chassis.

## **6.9           POWER UP AND START UP**

Applying power and starting up the ADD-32 should be done only by trained and qualified personnel. Familiarity with the hardware, the software, and the environment in which the equipment is to be applied is critical to safe and efficient system operation.

## **6.10          PULSE GENERATOR INSTALLATION**

Proper mechanical and electrical installation of the digital speed feedback device (Pulse Generator) is critical for optimum performance and reliability. Follow the instructions provided by the Pulse Generator manufacturer and system interconnection diagrams, if applicable.

The Maxi System Board Block Diagram, provided earlier in this section, shows pulse generator ("Tach") connection terminals. In addition, for Avtron SMARTach™ pulse generators (models M285, M485, and M685), the following figure shows how the tach alarm output should be connected to an ADD-32 drive.

Particular care should be exercised in selecting the shaft coupling. Use a zero backlash, Thomas Miniature Flexible or equivalent. When axial endplay exceeds  $\pm 0.020$ ", use Thomas CCX or equivalent. Do not use a helical spring type or rubber element type coupling.

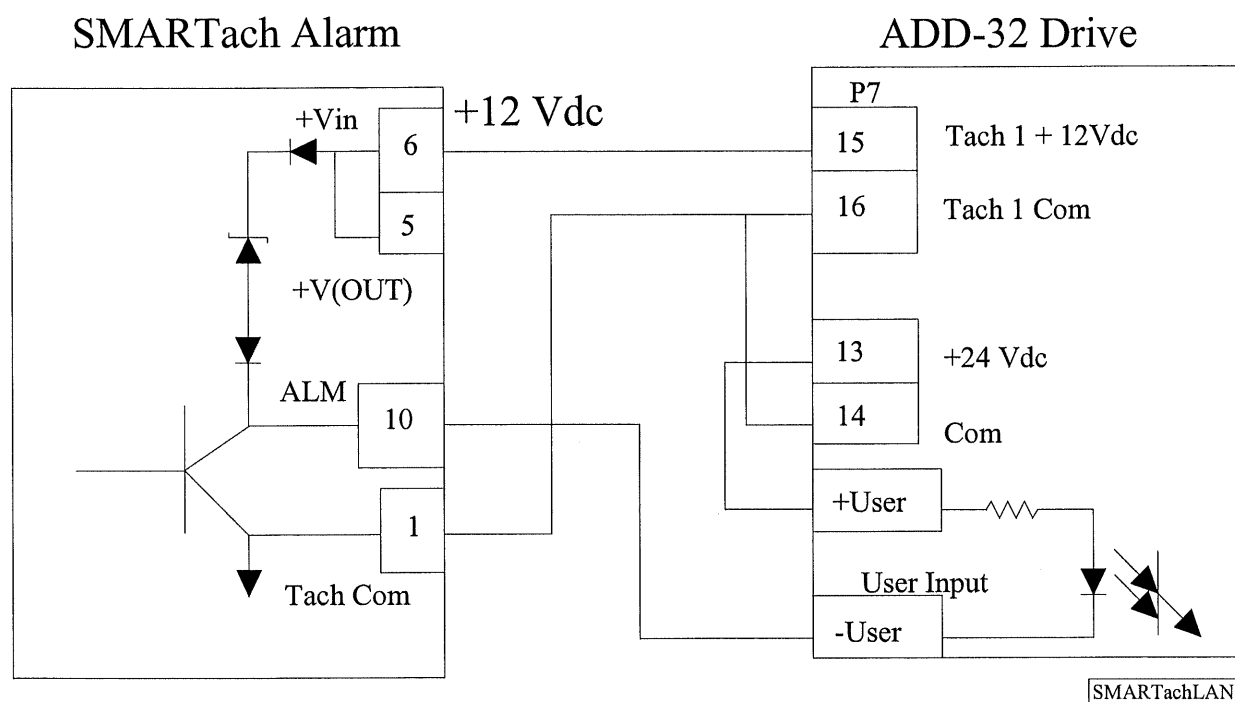


Figure 6-12. SMARTach Alarm Connections



# ESD PRECAUTIONARY GUIDELINES

## C A U T I O N

Certain circuit card assemblies and their components, typically integrated circuits, may be damaged by seemingly undetectable electrostatic discharge (ESD). Care must be exercised during handling/repair of these items. Use electrostatic discharge precautionary procedures.

The following guidelines are not necessarily all inclusive but rather serve as reminders for good shop practices for the handling/repair of ESD sensitive circuit card assemblies and devices.

- . Store ESD sensitive items in their original containers. These items are often marked with the symbol shown at the top of this page.
- . Put on a grounded wrist strap before handling any ESD sensitive item.
- . Clear work area of Styrofoam®, plastic, and vinyl items such as coffee cups.
- . Handle ESD items by the body, never the open edge connectors.
- . Never slide ESD sensitive items over any surface.
- . Transport ESD sensitive items in a static shielding container to a static-free work station.
- . If a static-free work station is not available, ground the transport container before removing or inserting an ESD item.
- . Electric tools used during repair should be grounded. For example, use only anti-static type solder suckers and grounded tip soldering irons. Discharge non-electric tools before use.
- . Pack ESD items in static shielding containers before shipping them to Avtron for repair.

\* Styrofoam® is a registered trademark of Dow Chemical.



## **SECTION VII**

# **MAINTENANCE AND TROUBLESHOOTING**

\*\*\*\*\*

### **W A R N I N G**

**THIS EQUIPMENT CONTAINS HAZARDOUS VOLTAGES. AVOID LOSS OF LIFE, SEVERE PERSONAL INJURY, OR PROPERTY DAMAGE BY FOLLOWING THE INSTRUCTIONS CONTAINED IN THIS MANUAL.**

**THE CONTROLLER PANEL CONTAINS HAZARDOUS VOLTAGES WHEN THE MAIN DRIVE CONTACTOR IS OPEN. THE POWER COMPONENTS, BRIDGE INTERFACE, SNUBBER, FIRING, AND VOLTAGE ISOLATION BOARDS HAVE CIRCUITS WHICH CONTAIN HAZARDOUS VOLTAGES.**

**TURN OFF AND LOCKOUT ALL POWER SOURCES AT THE FEEDER TO THE POWER CONVERTER BEFORE PERFORMING MAINTENANCE OR REPAIR. BEWARE OF "FOREIGN" EXTERNAL POWER SOURCES WHICH MAY STILL BE LIVE ALTHOUGH THE MAIN AC FEED IS OPENED.**

**ONLY QUALIFIED PERSONNEL SHOULD PERFORM THE FOLLOWING PROCEDURES ON THIS EQUIPMENT DUE TO THE COMPLEXITY OF THE ADD-32 POWER CONVERTER. PERSONNEL SHOULD BE FAMILIAR WITH ALL SAFETY NOTICES, INSTALLATION, OPERATION AND MAINTENANCE PROCEDURES IN THE MANUAL PRIOR TO WORKING ON THE ADD-32.**

\*\*\*\*\*

## 7.1 MAINTENANCE REQUIREMENTS

Proper maintenance of the ADDvantage-32 and its associated motor and process equipment is required. Refer to the instructions supplied with the motor and associated process equipment for proper maintenance procedures.

### PERIODIC MAINTENANCE

Under normal operating conditions, the ADDvantage-32 requires minimal periodic maintenance. The unit should be checked periodically for dirt accumulation within the enclosure. Regularly clean or replace filters on low pressure clean air source ventilation openings. Wire terminations on the power converter should be checked periodically for tightness.

To minimize downtime in the event of a component failure, spare parts should be stocked at the installation site. Refer to the spare parts list in the supplemental drawing package for recommendations on stocking of spare parts.

Use the following checklist for periodic maintenance.

1. Keep unit free from dirt. Vacuum or use low pressure air to keep clean.
2. If cabinet is equipped with filters, keep them free of dirt.
3. Check for correct operation of heat sink fans.
4. Check wire terminations for tightness.

\*\*\*\*\*

### WARNING

**THE USE OF UNAUTHORIZED PARTS IN THE REPAIR OF THIS EQUIPMENT, OR TAMPERING BY UNQUALIFIED PERSONNEL MAY RESULT IN DANGEROUS CONSEQUENCES. AVOID LOSS OF LIFE, SEVERE PERSONAL INJURY OR EQUIPMENT DAMAGE BY FOLLOWING RECOMMENDED SAFETY AND REPAIR PROCEDURES.**

\*\*\*\*\*

## 7.2

## GENERAL DIAGNOSTIC FEATURES

The ADD-32 has an extensive fault and diagnostic check capability. Refer to Table 7-3 for a list of faults and warnings that can be detected. There is also a watchdog timer that is reset by the microprocessor under normal operation. If the processor fails to reset the timer, then the DOK contactor opens and a DOK fault indication is displayed. Although fault and diagnostics checks are frequently identified by the DOK (Drive OK) circuit, not all conditions will be caught. Examples of fault conditions that cannot be detected by the ADD-32 itself include, but are not limited to, the following:

**I/O including digital and analog.** A failure in the hardware associated with the inputs or outputs can occur on a chip level and not be detected.

**Broken or loose interconnection/wire.** There are several connections inside the ADD-32 including critical feedback signals and/or connections to I/O external to the ADD-32 that could fail.

**Memory failure after initial power up check.** The ADD-32 checks memory as part of initial power up diagnostics, but a subsequent failure may go undetected and result in unpredictable operation. The watchdog timer is included to guard against this, but cannot be guaranteed to catch all possible memory faults once initial power up checks are completed successfully.

**SCR failure after initial power up check.** The ADD-32 can be configured to check proper firing on initial start up. A subsequent failure of an SCR to gate for any reason cannot be detected until the next RUN command sequence.

The ADDvantage-32 uses built-in diagnostics which constantly monitor for faults which may occur in the controller, motor, or other external inputs. The diagnostic levels used to assist in troubleshooting are as follows:

1. INITIAL POWERUP CHECK

Upon powerup of the drive, the diagnostic test checks all boards, cables, and incoming power. During this test the 12 status LED's on the front panel illuminate simultaneously, then shut off one at a time. If a failure occurs during the test, the corresponding LED remains illuminated and a fault message appears on the display. Refer to Table 7-1 for definitions of the LED's and Table 7-2 for definitions and solutions to the powerup fault messages.

**NOTE**

Faults must be corrected to continue operation of the ADDvantage-32. There is a slight delay in operation while the powerup check is performed.

On non-LAN hardware, the LEDs will all flash on and off several times during powerup.

TABLE 7-1. LED DEFINITIONS

TITLE	COLOR	DEFINITION
+5 V POWER ON	Green	Lights when 5 VDC power is present.
RUNNING	Green	Lights when a command is given to close the motor contactor. Commands are RUN, JOG, or THREAD.
EMERG STOP OK	Green	Lights when emergency stop input is high and emergency stop reset has been pressed.
DRIVE READY	Green	Lights when all internal faults have been cleared and fault reset has been pressed. Drive ready and emergency stop inputs must be on to run the unit.
USER LED	Amber	Can be set by user to illuminate when a digital bit in the data table goes high.
CURRENT LIMIT	Amber	Lights during a positive or negative current limit. This is not a fault condition; therefore, when the unit goes out of limit, the LED turns off.
FWD BRIDGE ON	Amber	Lights when forward bridge is being fired. Should light during forward motoring or reverse regeneration.
REV BRIDGE ON	Amber	Lights when reverse bridge is being fired. Should light during reverse motoring or forward regeneration.
DRIVE FAULT	Red	Lights when any fault occurs which shuts down the unit. Remains lit until all faults are cleared.
FIELD LOSS	Red	Lights during an emergency stop on a field loss fault. Stays lit until fault is cleared.
IOC FAULT	Red	Lights during an emergency stop on an instantaneous overcurrent fault. Stays lit until fault is cleared.
PROCESSOR FAIL	Red	Lights when watchdog timer on microprocessor board times out.



TABLE 7-2. POWERUP MESSAGES

FAULT MESSAGE	PROBLEM	SOLUTION
SYS BD BUS CABLE MISSING	Microprocessor board unable to communicate with system board.	a. Check cable B20623 at J2 on system board. b. Replace system board. c. Replace microprocessor board.
SYS BD ANALOG CABLE MISSING	Microprocessor board missing analog information from system board.	a. Check cable B20622 at J3 of system board. b. Replace system board. c. Replace microprocessor board.
SYS BD POWER CABLE MISSING	Microprocessor board detects missing power on system board.	a. Check cable B20727 at J1 of system board. b. Replace system board. c. Replace microprocessor board.
PWR I/F BOARD CABLE MISSING	Microprocessor board getting incorrect information from power supply board.	a. Check cable B20726-1 at J4 of microprocessor board. b. Replace power supply board. c. Replace microprocessor board.
CHECK ARMATURE BRIDGE CABLES (540 ADC AND UP ONLY)	Open circuit detected in armature bridge interlock loop.	Check interconnect cables to and within armature bridge for loose connectors, etc.
CT/THERMISTOR CABLE MISSING	Bad thermistor or missing cable.	a. Check cables at J8 and J2 of bridge interface board. b. Replace thermistor RT1. c. Replace microprocessor board.
INIT THE PLL.... INIT FAIL	Cannot lock onto phase lock loop.	a. Refer to Table 7-4 under fault message PLL LOCK. b. Bypass to view keyboard by pressing all four buttons (↓, ↑, →, S) at the same time. Unable to pull in contactor until drive is reset.
DRIVE > 510 AMPS CHECK P/N CAL	Senses unit is set at > 510A, but Y***:DRIVE P/N is set < 510A.	a. Change Y***:DRIVE P/N to conform to hardware. b. Replace bridge interface board. c. Replace microprocessor board.
DRIVE < 540 AMPS CHECK P/N CAL	Senses the unit is set < 540A, but Y***:DRIVE P/N is set > 540A.	a. Change Y***:DRIVE P/N to conform to hardware. b. Replace bridge interface board. c. Replace microprocessor board.

TABLE 7-2. POWERUP MESSAGES (Cont.)

FAULT MESSAGE	PROBLEM	SOLUTION
EEPROM CHKSUM FAIL CODE	Stored checksum does not match actual checksum.	a. Displayed after software change. To default memory, press S. "CORRECT CHECKSUM ?" is displayed. Press down (no) arrow. "DEFAULT CAL DATA?" is displayed. Press up (yes) arrow. After the display is defaulted, remove power to reset the ADDvantage-32. b. If software was not changed, replace microprocessor board. c. Bypass the warning by pressing S. "CORRECT CHECKSUM ?" is displayed. Press up (yes) arrow.
EEPROM VERSION INCOMPATIBILITY	Stored cal data version does not match program version.	Must default calibration data to prevent erratic functioning. To default memory, press S. "CORRECT VERSION?" is displayed. Press down (no) arrow. "DEFAULT CAL DATA?" is displayed. Press up (yes) arrow. After the display is defaulted, remove power to reset the ADDvantage-32.

## 2. FAULTS AND WARNINGS

The faults and warnings alert the user to the condition of the drive and motor. Faults are conditions that can damage the motor or drive if the condition continues. To protect against damage, the drive opens the DOK (Drive OK) contact which in turn opens the motor contactor. All faults are level sensed and must be rectified before FAULT RESET can be pressed. Warnings occur when limits in the drive have been reached or when a fault is about to occur, allowing the user to correct the condition before a drive fault occurs.

**Fault Queue** - The fault queue stores the last sixteen faults using a FIFO method of data storage. The FIFO faults reside in RAM and if a power loss occurs, the faults are saved in EEPROM. The FIFO stores all faults and issues a FLT CLEARED message indicating that the operator cleared the fault but not the FIFO memory. To reset the Fault Queue, set the CLR FLT QU bit to logic 1.

TYPES OF WARNINGS AND FAULTS

- A. Hardcoded Faults and Warnings - Hardcoded faults are not user-definable. Some hardcoded events are only valid when the motor contactor is picked up. See Table 7-3 for a list of faults, warnings, and motor contactor status. See Table 7-4 for fault messages and corrective action.
- B. User Defined Faults/Warnings - There are eight possible user defined fault messages which may be configured to any digital data point. The defined faults are Y\*\*\*:USR FAULT 1 through Y\*\*\*:USR FAULT 8. The label of the digital data point the user fault is configured for is shown in the fault FIFO.

TABLE 7-3. HARDCODED FAULTS AND WARNINGS

FAULT MESSAGE	FAULT (F) OR WARNING (W)	MOTOR CONTACTOR MUST BE PICKED UP?
A/D OFFSET	F	N
A/D REF RD	F	N
A/D SPAN	F	N
A/D ZERO RD	F	N
BRIDGE (II) T	F	Y
CNTL POWER	F	N
DRIVE CAL INCOMPATIBILITY	F	N
EEPRM WRITE	W	N
EEPROM CHECKSUM FAIL CODE XX	F	N
EEPROM VERSION INCOMPATIBILITY	F	N
FIELD LOSS	F	N
FLD CTL LOS	W	N
FLT CLEARED	W	N
GATE POWER	F	N
INST OVR CU	F	Y
INVALID A/D	F	N
L-FREQ HIGH	F	N
L-FREQ LOW	F	N
LINE VOLTAGE	F	N

TABLE 7-3. HARDCODED FAULTS AND WARNINGS (Cont.)

FAULT MESSAGE	FAULT (F) OR WARNING (W)	MOTOR CONTACTOR MUST BE PICKED UP?
MOTOR (II) T	F	Y
MOTOR STALL	F	Y
MOTOR TEMP	F	N
OPEN ARM	F	Y
OPEN SYS CBL	F	N
PHASE IMBAL	F	N
PHASE LOSS	F	N
PLL LOCK	F	N
SCR OPN A+F	F	Y
SCR OPN B+F	F	Y
SCR OPN C+F	F	Y
SCR OPN A-F	F	Y
SCR OPN B-F	F	Y
SCR OPN C-F	F	Y
SCR OPN A+R	F	Y
SCR OPN B+R	F	Y
SCR OPN C+R	F	Y
SCR OPN A-R	F	Y
SCR OPN B-R	F	Y
SCR OPN C-R	F	Y
SCR SHRT A+	F	N
B+	F	N
C+	F	N
A-	F	N
B-	F	N
C-	F	N
SINK TEMP	F	N
TUNE FAULT	F	Y
TUNE PASS	F	Y
USER 1-8 FLT	F	-

TABLE 7-4. FAULT DESCRIPTIONS

FAULT MESSAGE	PROBLEM	SOLUTION
A/D OFFSET	Bad auto offset. Adjust on analog inputs.	Replace microprocessor board.
A/D REF RD	Bad auto span.	Replace micro board.
A/D SPAN	Bad auto span. Adjust on analog inputs.	Replace microprocessor board.
A/D ZERO RD	Bad auto offset.	Replace micro board.
BRIDGE (II) T	Heatsink overtemperature.	a. Undersized motor. b. Parameter X001: MOTOR IARM scaled wrong. c. Parameter X002: MOTOR IFLD scaled wrong. d. Check bearings. e. Check gearbox oil. f. Replace bridge interface board. g. Replace micro board.
CNTL POWER	Loss of power to the unit.	a. If only fault, check plant power. b. Check other faults.  <b>NOTE:</b> CNTL POWER will appear in FIFO if power is cycled.
DRIVE CAL INCOMPATIBILITY	Calibration and configuration data not compatible with drive software.	Default drive and enter cal and config.
EEPRM WRITE	Noncritical fault. Check calibration parameters for bad data.	Replace microprocessor board.
EEPROM CHECKSUM FAIL CODE XX	Checksum error.	Replace micro board.
EEPROM VERSION INCOMPATIBILITY	Checksum error.	a. Default drive and enter cal and config. b. Replace micro board.

FAULT MESSAGE	PROBLEM	SOLUTION
FIELD LOSS	Field current feedback low or missing.	a. Check parameter X***:MOTOR I FLD for proper motor/drive ratio. b. Check field wiring. c. Check for field jumpers at TB1 (3-5) and (4-6). d. Check fuses F1 and F2. e. Check FLD I ECON percentage. (50% recommended) f. Check field ohms. (100-300 ohms) g. Replace bridge interface board. h. Replace power module.
FLD CTL LOS	Field cannot reach setpoint.	a. Check for proper MOTOR IFLD value. b. Check for low line voltage causing field firing into MIN ALPHA LIMIT. c. Check for proper FLD MAX LMT value. d. Replace bridge interface board. e. Replace microprocessor board.
FLT CLEARED	Faults have been manually cleared.	N/A
GATE POWER	No gate power available or gate power present when it should be inhibited.	a. Replace bridge interface board. b. Replace microprocessor board.
INST OVR CU	Instantaneous Overcurrent-Armature Current above 300%.	a. Retune unstable current loop. b. Check for shorted motor armature. c. Check for stable line voltage. d. Replace bridge interface board. e. Replace microprocessor board. f. Replace base.
INVALID A/D	Calibration parameter I/O V-REF out of limits.	a. Correct calibration. b. Replace microprocessor board.
L-FREQ HIGH	Line frequency above 63 Hz.	a. Check plant power frequency. b. Replace power supply board. c. Replace microprocessor board.
L-FREQ LOW	Line frequency below 43 Hz.	a. Check plant power frequency. b. Replace bridge interface board. c. Replace microprocessor board.
LINE VOLTAG	Low line voltage.	Measure incoming voltage.

FAULT MESSAGE	PROBLEM	SOLUTION
MOTOR (II) T	Motor overtemperature due to armature current above 110% for too long.	<ul style="list-style-type: none"> <li>a. Undersized motor.</li> <li>b. Parameter X001: MOTOR IARM scaled wrong.</li> <li>c. Parameter X002: MOTOR IFLD scaled wrong.</li> <li>d. Check bearings.</li> <li>e. Check gearbox oil.</li> <li>f. Replace bridge interface board.</li> <li>g. Replace micro board.</li> </ul>
MOTOR STALL	Motor failed to move with armature current.	<ul style="list-style-type: none"> <li>a. Check setup of stall parameters.</li> <li>b. Check for mechanical binding.</li> <li>c. Check for correct armature and field current scaling.</li> <li>d. Check for correct speed feedback.</li> <li>e. Replace motor.</li> </ul>
MOTOR TEMP	Motor Thermal Overload-Armature Current above 100% for more than rated time.	<ul style="list-style-type: none"> <li>a. Enable P***:BYPASS I2R to auto phase back current limits.</li> <li>b. Check for proper field current.</li> <li>c. Check for a mechanical problem causing excess currents.</li> <li>d. Check for proper current limit settings.</li> </ul>
OPEN ARM	No armature resistance detected or more than four SCR's failed.	<ul style="list-style-type: none"> <li>a. Check armature wiring.</li> <li>b. Check motor for open armature through 360° rotation.</li> <li>c. Check fuse F11 for 4 quad drives.</li> <li>d. Check for motor contactor closing.</li> <li>e. Replace bridge interface board.</li> </ul>
OPEN SYS CBL	Senses missing cable between microprocessor board and system board.	<ul style="list-style-type: none"> <li>a. Check cable B20623.</li> <li>b. Replace system board.</li> <li>c. Replace microprocessor board.</li> </ul>
PHASE IMBAL	Line voltage unstable, varies over 10%.	<ul style="list-style-type: none"> <li>a. Check incoming line voltage.</li> <li>b. Check line fuses.</li> <li>c. Check for excessive line notching.</li> <li>d. Replace bridge interface board.</li> </ul>
PHASE LOSS	Line power missing.	<ul style="list-style-type: none"> <li>a. Check fuses F8, F9, and F10.</li> <li>b. Check incoming line voltage.</li> <li>c. Check for excessive line notching.</li> <li>d. Replace bridge interface board.</li> </ul> <p><b>NOTE:</b> PHASE LOSS will appear in FIFO if power is cycled.</p>

FAULT MESSAGE	PROBLEM	SOLUTION
PLL LOCK	Cannot lock onto line frequency.	a. Check line frequency. b. Check for notching. c. Check fuse F10. d. Check cable J3 on bridge interface board. e. Check cable J1 on the snubber board. f. Replace cable between bridge board J4 and micro board J3. g. Replace bridge board. h. Replace micro board.  <b>NOTE:</b> PLL LOCK will appear in FIFO if power is cycled.
SCR OPN A+F	A + open SCR fault message. SCR CR1 or fuse F8 for 510 amp and below. SCR-A101 or fuse F1 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN B+F	B + open SCR fault message. SCR CR2 or fuse F9 for 510 amp and below. SCR-A102 or fuse F2 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN C+F	C + open SCR fault message. SCR CR3 or fuse F10 for 510 amp and below. SCR A103 or fuse F3 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN A-F	A - open SCR fault message. SCR CR4 or fuse F8 for 510 amp and below. SCR A104 or fuse F4 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.



FAULT MESSAGE	PROBLEM	SOLUTION
SCR OPN B-F	B - open SCR fault message. SCR CR5 or fuse F9 for 510 amp and below. SCR A105 or fuse F5 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN C-F	C - open SCR fault message. SCR CR6 or fuse F10 for 510 amp and below. SCR A106 or fuse F6 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN A+R	Open SCR fault message. SCR CR1 or fuse F8 for 510 amp and below. SCR A101 or fuse F1 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN B+R	Open SCR fault message. SCR CR2 or fuse F9 for 510 amp and below. SCR A102 or fuse F2 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN C+R	Open SCR fault message. SCR CR3 or fuse F10 for 510 amp and below. SCR A103 or fuse F3 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN A-R	Open SCR fault message. SCR CR4 or fuse F8 for 510 amp and below. SCR A104 or fuse F4 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.

FAULT MESSAGE	PROBLEM	SOLUTION
SCR OPN B-R	Open SCR fault message. SCR CR5 or fuse F9 for 510 amp and below. SCR A105 or fuse F5 for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR OPN C-R	Open SCR fault message. SCR CR6 or fuse F10 for 510 amp and below. SCR A106 or fuse for 540 amp and above bridges.	a. Check fuse. b. Check cable assembly connected to J3 of microprocessor board and its associated connectors. c. Replace SCR or drive base assembly. d. Replace bridge interface board. e. Replace microprocessor board.
SCR SHRT A+	Shorted SCR-CR1 or snubber on 510 ADC and below units or Shorted SCR-A101 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.
SCR SHRT B+	Shorted SCR-CR2 or snubber on 510 ADC and below units or Shorted SCR-A102 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.
SCR SHRT C+	Shorted SCR-CR3 or snubber on 510 ADC and below units or Shorted SCR-A103 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.
SCR SHRT A-	Shorted SCR-CR4 or snubber on 510 ADC and below units or Shorted SCR-A104 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.
SCR SHRT B-	Shorted SCR-CR5 or snubber on 510 ADC and below units or Shorted SCR-A105 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.

FAULT MESSAGE	PROBLEM	SOLUTION
SCR SHRT C-	Shorted SCR-CR6 or snubber on 510 ADC and below units or Shorted SCR-A106 on 540 ADC and above units	a. Replace bridge interface board and snubber board if applicable. b. Replace SCR module. c. Replace microprocessor board.
SINK TEMP	Heat sink > 65°C.	a. Allow drive to cool. b. Replace thermistor RT1. c. Replace bridge interface board. d. Replace microprocessor board.
TUNE FAULT	Self tune failed.	a. Self tune aborted by operator. b. Run removed. c. Motor/Drive not compatible; must manually tune. d. Iarm cont > 80%. Check Iarm feedback wires at bridge board for correct polarity. If correct, manually tune.
TUNE PASS	Self tune routine has passed.	Remove the run and clear the fault.
USER 1-8 FLT	Digital bit configured to Y:XXX parameter. USER FLT X has gone high (1).	Check configuration for USER FLT X.
XXXXXXXXXXXX	DPB: Label configured to USER FAULTS 1-8.	Check function of software block that causes the output bit to go high.

### 3. SIGNAL ANALYZER

The Signal Analyzer (refer to Section V) also assists the user in diagnosing failures. The analyzer can record four parameters over a specified time period, which is useful in detecting machine or system problems. For example, speed feedback can be recorded to detect a bad gear tooth or out of balance roll. Refer to Section V for setup and operation of the signal analyzer.

### 4. FTYPE FAILURE TYPE PROCEDURES

If a FTYPE failure occurs, the following procedure should be followed to gather the information needed for Avtron to solve the fault.

Typical Display:

Ftype:02 sub:01  
AT: FFFF81D0

- a. Copy ALL information accurately on initial FTYPE DISPLAY -- BOTH LINES!!
- b. PRESS the UP ARROW KEY very briefly. You should see the following display with the "AT" replaced by a level number in parenthesis. If you do not see a (1), then press the DOWN ARROW KEY to get back to the "AT" and try again.

Ftype:02 sub:01  
(1) 800271C4

- c. When the (1) level is displayed, copy down the lower line of the display (the level and the number to the right of the level).
- d. AGAIN, briefly press the UP ARROW KEY and step to level 2 as shown:

Ftype:02 sub:01  
(2) 80027484

- e. When the (2) level is displayed, copy down the lower line of the display.
- f. Press the UP ARROW key to view levels 3, 4, 5, 6. Copy down the level and the number to the right of the level for each level.
- g. FAX/EMAIL the DRIVE HARDWARE and DRIVE SOFTWARE part numbers and all information collected above to Avtron for evaluation.

## 7.3 BOARD REPLACEMENT

\*\*\*\*\*

### CAUTION

**THE ADDvantage-32 PC BOARDS CONTAIN COMPONENTS WHICH MAY BE DAMAGED BY ELECTROSTATIC DISCHARGE (ESD). EXERCISE CARE DURING HANDLING/REPAIR OF THESE BOARDS.**

\*\*\*\*\*

#### 7.3.1 REPLACING MICROPROCESSOR BOARD (A1) (Refer to Figure 7-1.)

1. Record all calibration and configuration data.
2. Remove power from the unit.
3. Open front cover.
4. Remove all cables (J1-J4) from microprocessor board.
5. Remove ground wire.
6. Slide front cover (with microprocessor board) up and off the hinges.
7. Attach new cover and microprocessor board to the unit.
8. Replace ground wire.
9. Replace all four cables and close the door.
10. Reapply power and re-enter data.
11. Reset unit.
12. Measure voltage across TP1 and TP2. Enter value into X\*\*\*:I/O V-REF.

#### 7.3.2 REPLACING SYSTEM BOARD (A2) (Refer to Figure 7-1.)

1. Remove power from the unit.
2. Open front cover.
3. Remove cables (J1-J6) from system board.
4. Remove all four cables from microprocessor board.
5. Remove ground wire.
6. Detach cover and microprocessor board from unit.
7. Open base assembly door.
8. Detach system board by removing the four screws located on the inside of the door.
9. Attach new system board and case.
10. Replace ground wire.
11. Close door and attach the microprocessor board.
12. Reconnect all four cables on microprocessor board and all six cables on the system board.
13. Close cover and reapply power.

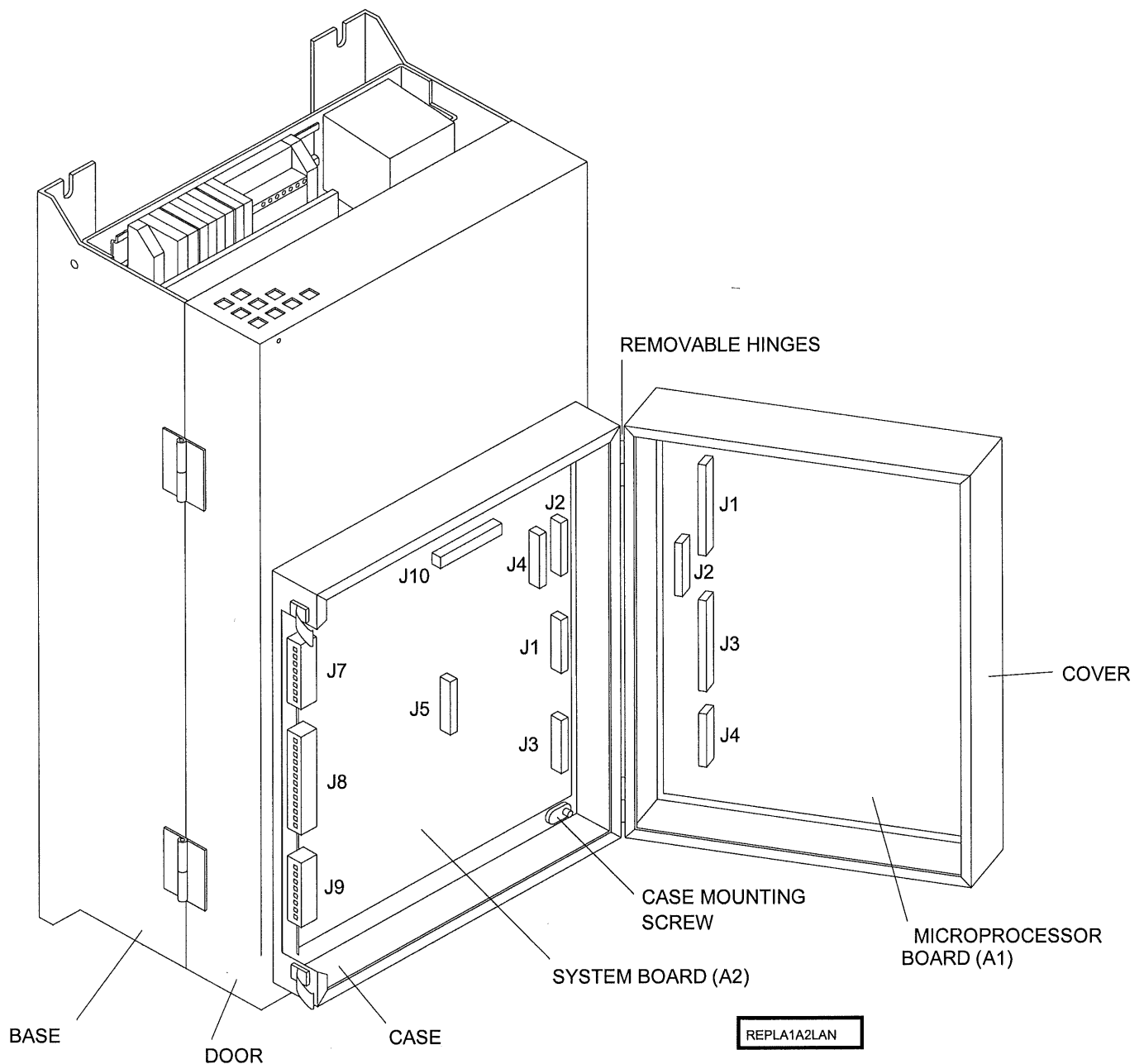


Figure 7-1. Replacing System and Microprocessor Boards

**NOTE**

Replacement of the system and microprocessor boards is the same for all ADDvantage-32 units, regardless of size.

### 7.3.3 REPLACING BRIDGE INTERFACE BOARD (A3) AND SNUBBER BOARD (A4) (510 ADC and Below) (Refer to Figures 7-2 and 7-5.)

1. Remove power from the unit.
2. Open base assembly door.
3. Remove cables on bridge interface board.
4. Loosen the two captive screws that secure the bridge interface assembly to the chassis. Swing the assembly out on its hinges.
5. Remove ground wire.
6. Remove J1 from snubber board (A4).
7. Slide bridge interface assembly off the hinges by lifting upward.
8. Place new assembly on hinges.
9. Replace ground wire.
10. Reconnect J1 cable to snubber board.
11. Tighten two captive screws to hold bridge interface assembly in place.
12. Replace seven cables on bridge interface board and shut the base assembly door.
13. Reapply power to the unit.

### 7.3.4 REPLACING BRIDGE INTERFACE BOARD (A3) AND SNUBBER BOARD (A4) (550 ADC) (Refer to Figure 7-3.)

1. Remove power from the unit.
2. Open the main drive door.
3. Remove cables on bridge interface board.
4. Remove ground wire by pulling off the push-on terminal, located near J3.
5. Loosen the two captive screws that secure the bridge interface assembly to the chassis. Carefully raise the assembly up about 1/4" and then away from the base, so that the two tabs at the top separate from the slots.
6. Remove J1 from snubber board (A4).
7. Reconnect J1 cable to new snubber board.
8. Place the new bridge interface assembly in position and insert the two tabs at the top into the slots on the base.
9. Tighten two captive screws to hold bridge interface assembly in place.
10. Replace ground wire.
11. Replace seven cables on bridge interface board and shut the main drive door.
12. Reapply power to the unit.

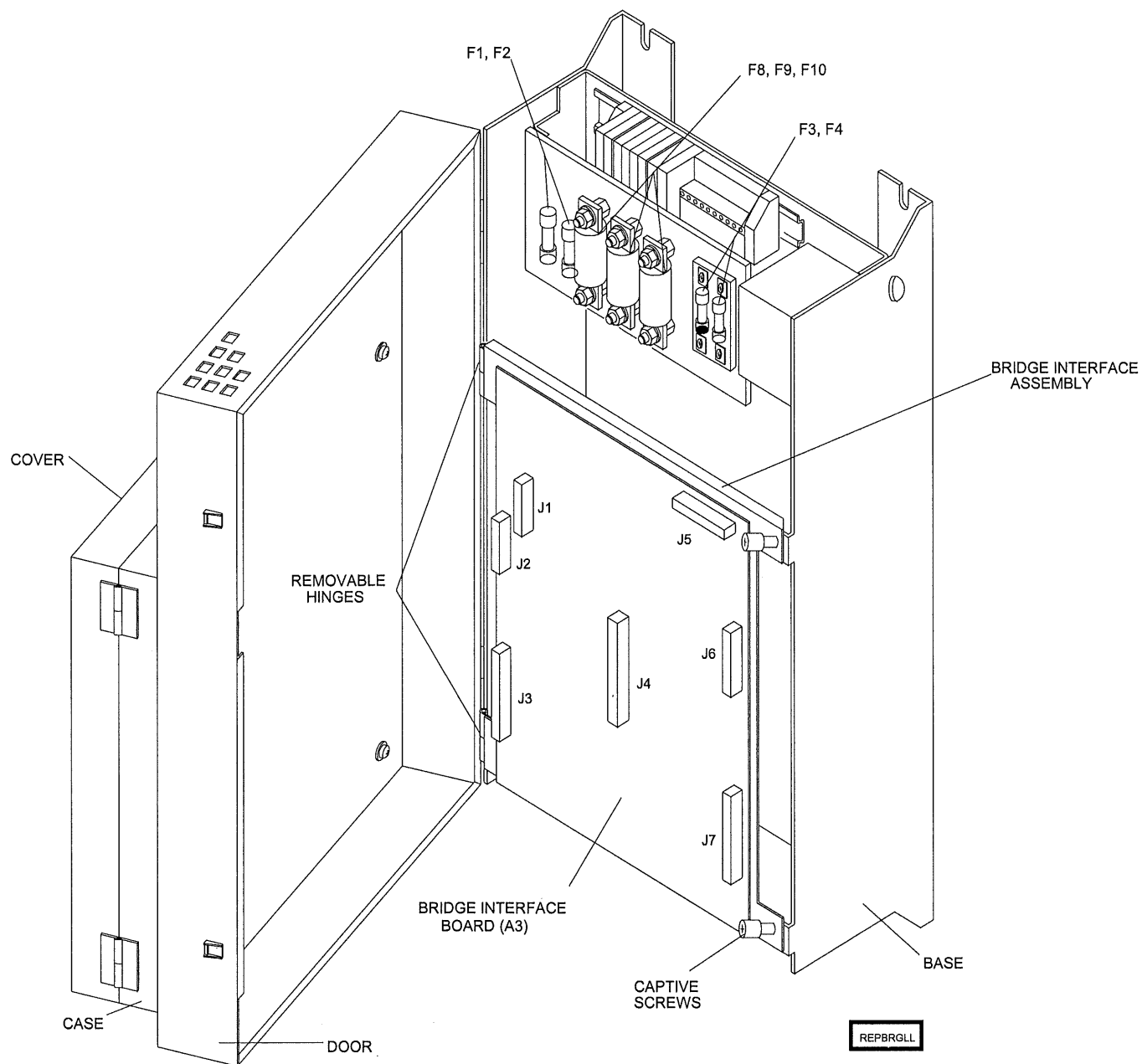


Figure 7-2. Replacing Bridge Interface Board  
(510 ADC and Below)



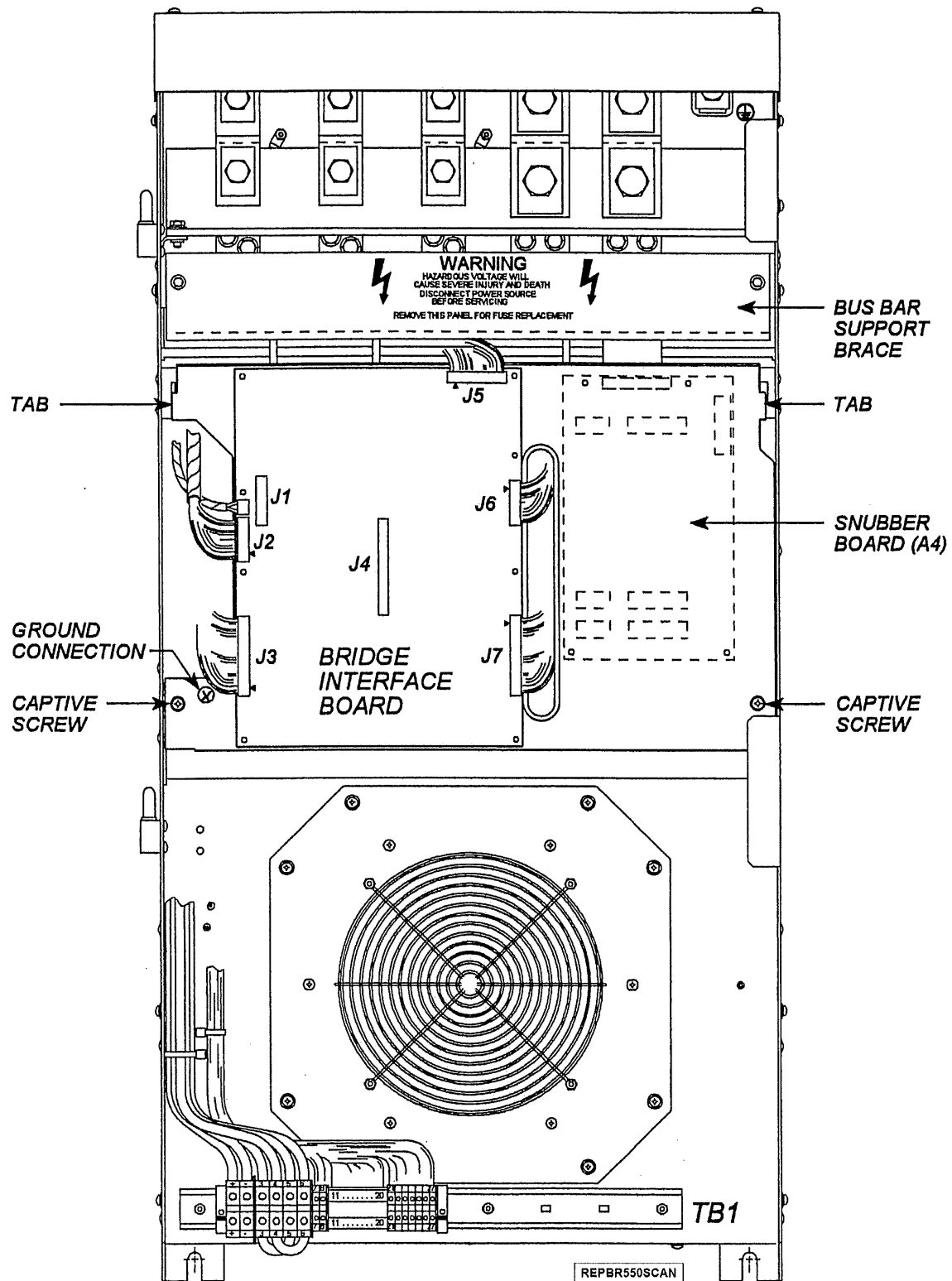


Figure 7-3. Replacing Bridge Interface Board (550 ADC)

## 7.3.5

**REPLACING BRIDGE INTERFACE BOARD (A3) (540, 850, 1550, and 3000 ADC)**  
(Refer to Figure 7-4.)

1. Remove power from the unit.
2. Disconnect armature bridge cables from J2 and J3.
3. Open base assembly door.
4. Remove ground wire.
5. Remove cables on bridge interface board.
6. Loosen the two captive screws holding the bridge interface assembly to the base.
7. Slide bridge interface assembly off the hinges.
8. Install new assembly on hinges.
9. Reconnect ground wire to the bottom left of the front panel.
10. Tighten two captive screws to hold bridge interface assembly in place.
11. Replace four cables to bridge interface board and shut the drive door.
12. Connect armature bridge cables to J2 and J3.
13. Reapply power to the unit.

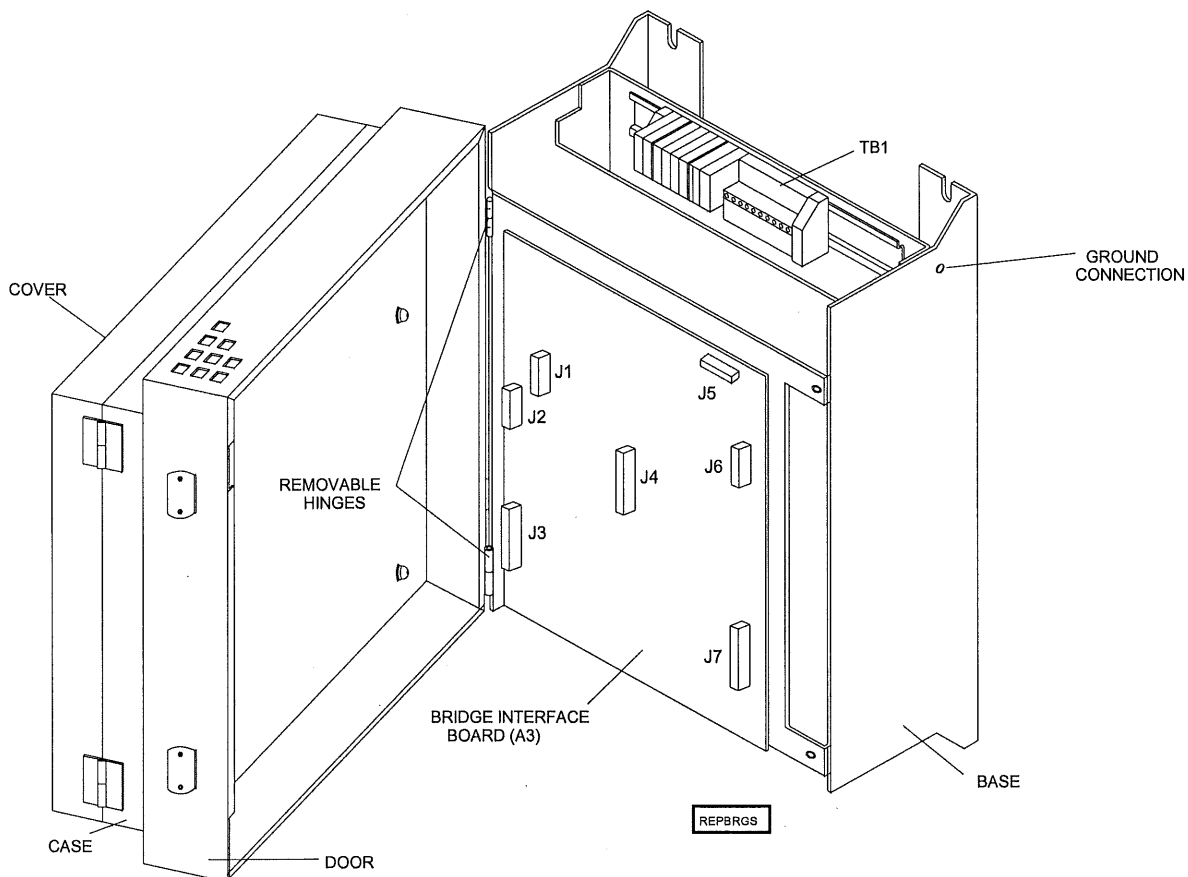


Figure 7-4. Replacing Bridge Interface Board  
(540, 850, 1550, and 3000 ADC)

## 7.4

**REPLACING DRIVE SUB-ASSEMBLY (510 ADC and Below)**

(Refer to Figure 7-5.)

\*\*\*\*\*

**WARNING**

**HAZARDOUS VOLTAGES WHICH CAN CAUSE SEVERE INJURY OR DEATH ARE PRESENT DURING THE OPERATION OF THIS EQUIPMENT. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE MAKING ANY REPAIRS.**

\*\*\*\*\*

This procedure covers replacement of the entire DC Drive Controller Base Sub-Assembly. To replace individual power components, such as thyristors and fuses, see section 7.6.

1. Remove power from the unit.
2. Open front cover.
3. Remove system interconnections (J4, J5, J6) from system board, shown in Figure 7-1.
4. Close cover and open base assembly door.
5. Remove all cables from bridge interface board.
6. Remove ground wire from door.
7. Remove door with microprocessor board and system board from the base assembly.
8. Release two captive screws holding bridge interface assembly to the chassis. Swing assembly out on its hinges.
9. Remove ground wire from bridge interface assembly.
10. Remove snubber cable connector J1 located on back of bridge interface assembly.
11. Slide bridge interface assembly up and off of hinges.
12. Remove high voltage wiring at L1, L2, L3, A1, A2, and DB1.
13. Remove wiring from TB1 and GND.
14. Detach unit from panel.
15. Mount spare base assembly to panel using existing hardware.
16. Reattach wiring to TB1 and GND.
17. Reapply high voltage wiring.
18. Slide bridge interface assembly onto its hinges.
19. Replace ground wire on bridge interface assembly.
20. Attach snubber cable at J1 on back of bridge interface assembly.
21. Tighten two captive screws holding bridge interface assembly to base.
22. Slide door on the base assembly.
23. Replace ground wire on door.
24. Attach all seven bridge interface cables and shut door.

25. Open cover and attach J4, J5, J6 to system board.
26. Verify all connections.
27. Reapply power.

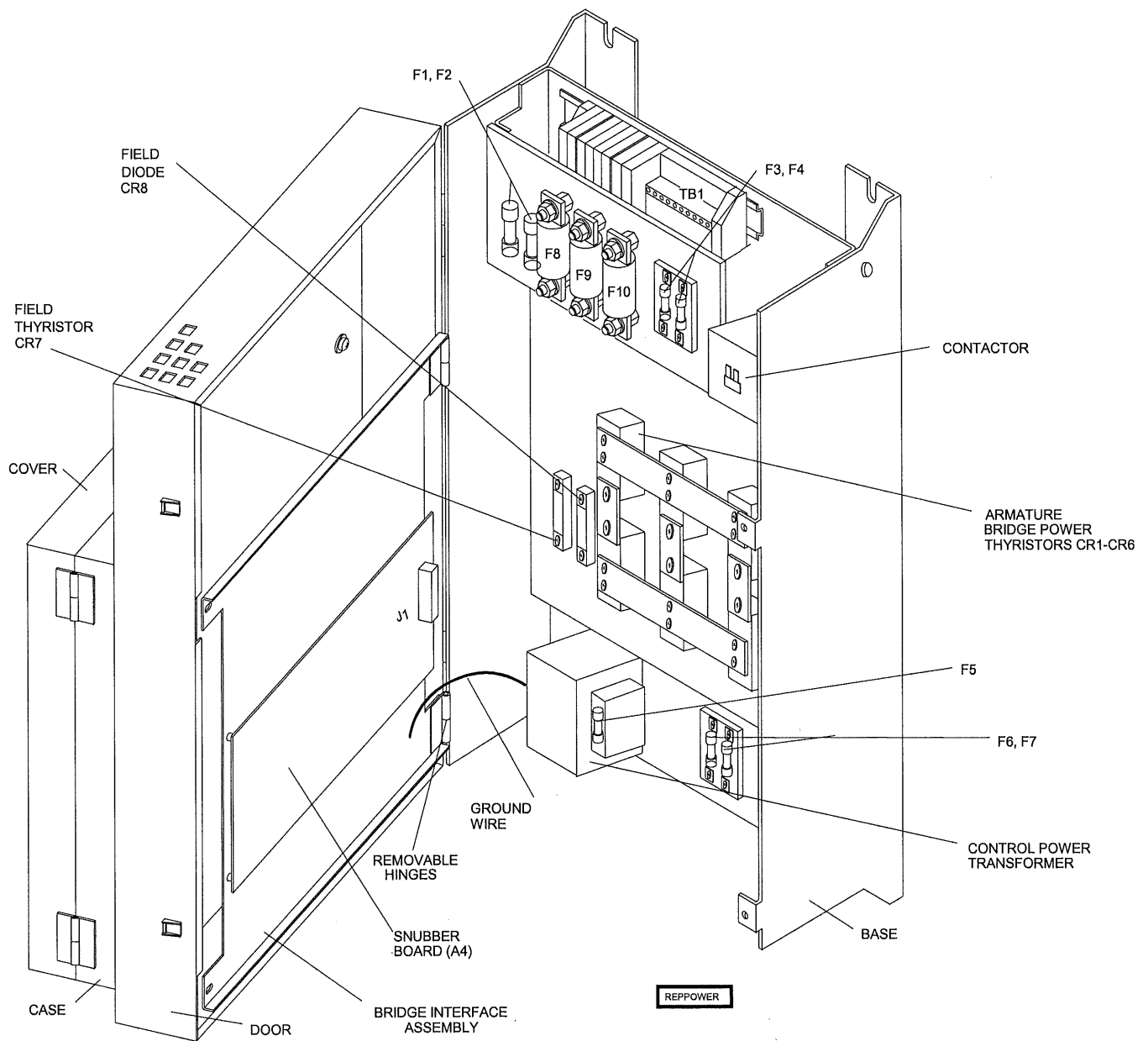


Figure 7-5. Replacing Power Components  
(510 ADC and Below Units)

## 7.5

## REPLACING DRIVE SUB-ASSEMBLY (550 ADC)

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## WARNING

**HAZARDOUS VOLTAGES WHICH CAN CAUSE SEVERE INJURY OR DEATH ARE PRESENT DURING THE OPERATION OF THIS EQUIPMENT. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE MAKING ANY REPAIRS.**

\*\*\*\*\*

This procedure covers replacement of the entire DC Drive Controller Base Sub-Assembly. To replace individual power components, such as thyristors and fuses, see Section 7.7.

1. Remove power from the unit.
2. Open the front controller housing cover.
3. Refer to Figures 7-1, 7-3, and 7-6. Remove system interconnections from the system board, shown in Figure 7-1. Close cover.
4. Open the main drive door.
5. Remove all cables from the bridge interface board (see Figure 7-3).
6. Remove ground wire from the door.
7. Remove the door, with microprocessor board and system board in the controller attached, from the base assembly. Set aside for reuse later.
8. Remove the bridge interface, as instructed in paragraph 7.3.4. Set aside for reuse later.
9. Remove high voltage wiring at L1, L2, L3, A1, and A2.
10. Remove wiring from TB1 and GND.
11. The complete sub-assembly may now be removed and replaced. Use existing hardware.
12. Reattach wiring to TB1 and GND.
13. Reattach high voltage wiring at L1, L2, L3, A1, and A2.
14. Reinstall the bridge interface from step 8 (see paragraph 7.3.4).
15. Replace the door/controller from step 7.
16. Replace ground wire on door.
17. Attach all seven bridge interface cables and shut door.
18. Open cover and attach system connections to the system board.
19. Verify all connections.
20. Close cover and reapply power.

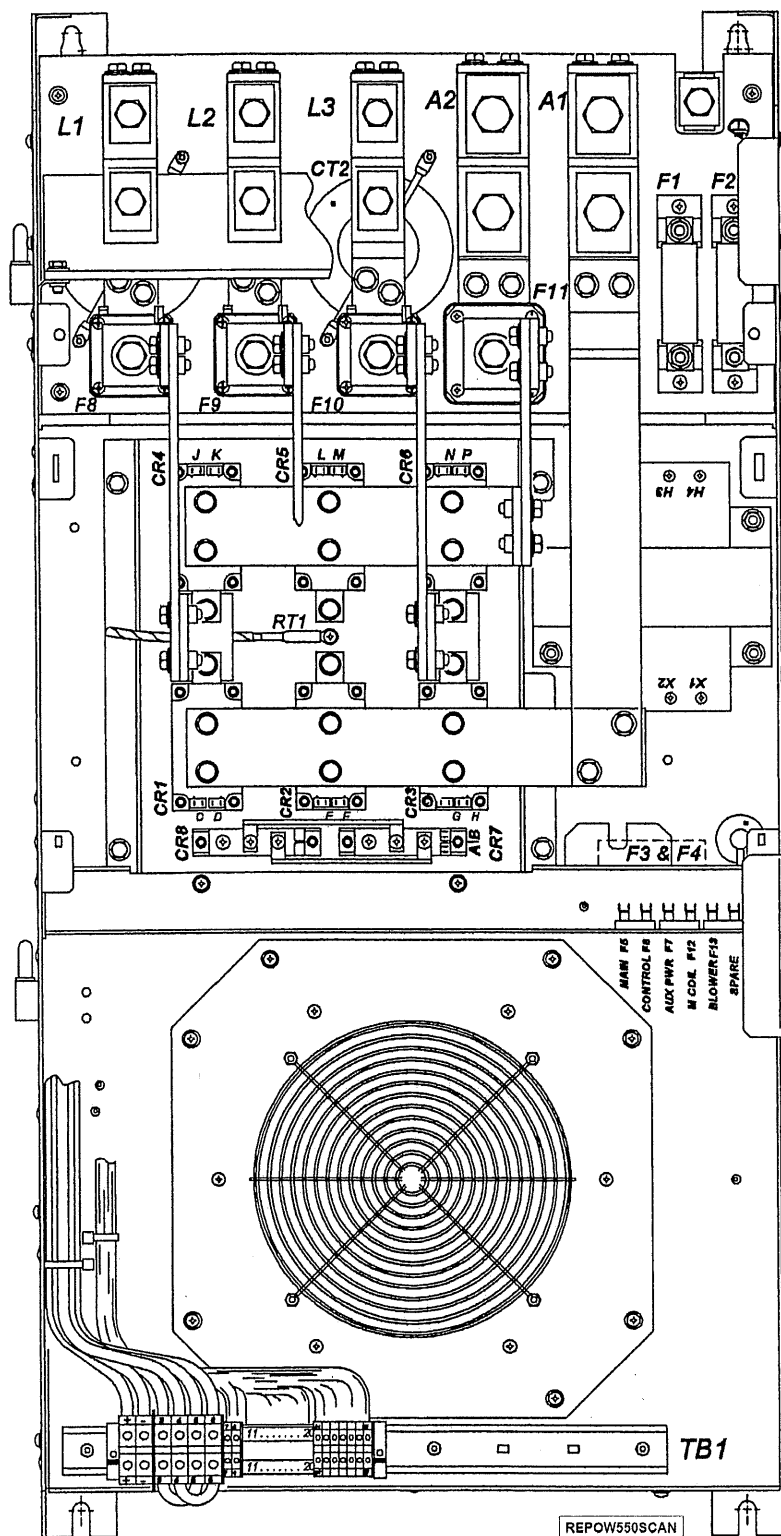


Figure 7-6. Replacing Power Components (550 ADC)

## 7.6

## TEST PROCEDURE FOR LEAKING THYRISTORS/SCRs

An SCR might be leaky or shorted if a false Tach Loss and/or SCR SHRTX  $\pm$  fault occurs when the DC contactor closes. To determine this, perform the following steps:

1. From the main keyboard/display menu, use the up and down arrow keys until "OPERATE" is displayed.
2. Press the right arrow key and "DRIVE ANALOG" will be displayed.
3. Press the right arrow key again and "A000 FIL SPEED" will be displayed.
4. Press the up arrow key until "A012 ARM VOLTS" is displayed. Verify that the section is stopped and the DC contactor is open. If the voltage is above 10 or 20 volts, an SCR may be leaking. If an SCR is shorted significantly, the drive diagnostics should fault out on power up. The FAULT FIFO should indicate which SCR is bad.

The diagnostics may indicate a shorted SCR at drive power up that may actually be the leaking SCR; it may be identified as follows:

SCR SHRT A+	CR1	SCR SHRT A-	CR4
SCR SHRT B+	CR2	SCR SHRT B-	CR5
SCR SHRT C+	CR3	SCR SHRT C-	CR6

On the other hand, the fault diagnostics may not be able to reliably determine exactly which SCR is leaking. For a leaking SCR, the fault diagnostics are clearable and the drive will run without blowing the 3-phase line fuses. **A shorted SCR will cause one or two 3-phase line fuses to blow.** The following test should be done to make sure FAULT FIFO has correctly identified the shorted SCR or to identify a leaky SCR.

1. Power off the drive.
2. Open the drive to access the Bridge Interface board.
3. Disconnect all the removable connectors on the board and swing open the panel to expose the snubber board.
4. Disconnect the snubber board by removing the connector P1 on the snubber board. However, for large drives this may not be possible. Therefore, skip this step for drives 540 amperes and above.
5. Clip a lead from a DVM to SCR bus A1 (BA1) located on main base assembly.
6. Reconnect all cables on bridge interface board.
7. Power up drive (run off). Measure and record AC volts between BA1 and Phase A, Phase B, Phase C.
8. Turn power off to drive. Move clip lead from bus bar A1 to bus bar A2 (BA2) by first removing all the cables on the bridge interface board.
9. Reconnect cables on the Bridge interface board.
10. Power up drive with run off. Measure and record the AC volts between bus bar A2 and Phase A, Phase B, Phase C.

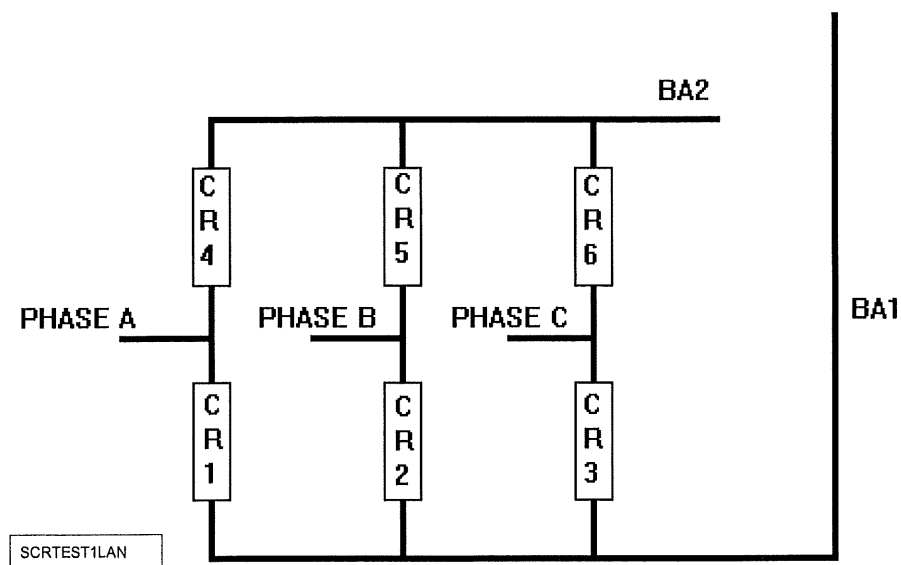


Figure 7-7. SCR Module Layout

The measured voltage that is significantly lower than all the others measured indicates a bad SCR and can be determined with the following table:

	<b>BA1</b>	<b>BA2</b>
<b>Phase A</b>	CR1	CR4
<b>Phase B</b>	CR2	CR5
<b>Phase C</b>	CR3	CR6

Example: Measured AC voltages (snubber disconnected)

	<b>BA1</b>	<b>BA2</b>
<b>Phase A</b>	285	230
<b>Phase B</b>	150	250
<b>Phase C</b>	327	243

The above table indicates CR2 is leaky.



**NOTE**

IF THE SNUBBER IS NOT DISCONNECTED, THE VOLTAGE DIFFERENCE MAY BE VERY SMALL.

Leaky SCRs on older style drives may require burden resistors. There are RESISTOR MODIFICATION KITS which are used as a burden on systems that have leaky SCRs. The resistors are standard now on newer drives, but on older drives may need to be added.

There are two different kits, the only differences being in the lugs provided. The resistors are 25K ohms, 50W and are connected across the armature circuit. The resistors bleed off SCR leakage so that false tach loss trips do not occur on the application of a run.

KIT P/N	INSTRUCTIONS	FOR USE ON
A22481	A22428	280, 360, and 510 Amp DC Drives
A22374	A22375	Most others. Check with factory.

**7.7****INDIVIDUAL SCR MODULE TEST**

An SCR module can be tested individually when removed from the drive. It is recommended that the SCR module be cold for this test and should not have been in operation for a considerable time preceding the test. Follow the steps below for each SCR on the module.

**USING AN ANALOG OHMMETER SET TO MEGOHM SCALE**

1. Measure the resistance between the Cathode and Anode. It should be 1M $\Omega$  or greater.
2. Reverse ohmmeter leads. It should again read 1M $\Omega$  or greater.
3. Connect positive lead of the ohmmeter to anode and negative lead to cathode. Jumper anode to gate. The resistance should now read less than 1K $\Omega$ .
4. Removing the jumper should indicate a reading of 1M $\Omega$  or greater on the ohmmeter.

Any variation of readings on the ohmmeter indicates a leaky, shorted, or open SCR.

**NOTE**

IN CASE OF A HOT SCR, THE READINGS MAY BE SIGNIFICANTLY LOWER IN STEPS 1, 2, AND 4.

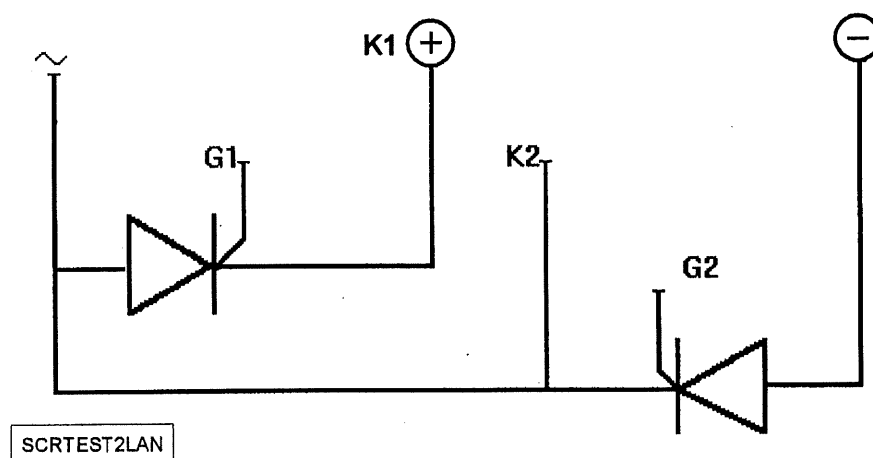


Figure 7-8. SCR Module Diagram

## 7.8 THYRISTOR/DIODE REPLACEMENT (510 ADC and Below)

\*\*\*\*\*

### WARNING

**HAZARDOUS VOLTAGES WHICH CAN CAUSE SEVERE INJURY OR DEATH ARE PRESENT DURING THE OPERATION OF THIS EQUIPMENT. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE MAKING ANY REPAIRS.**

\*\*\*\*\*

TABLE 7-5. SPECIAL TOOLS REQUIRED

QTY.	DESCRIPTION	USED ON DRIVE SIZES
1	1/4" Drive Torque Wrench (0-75 in-lb)	ALL
1	5/32" Hex Head Socket with Allen wrench insert bit (1/4" drive)	ALL
1	Hex Head Socket with #2 Phillips screwdriver insert bit (1/4" drive)	DC0010, DC0030, DC0056, DC0110
1	Hex Head Socket with #3 Phillips screwdriver insert bit (1/4" drive)	DC0180, DC0280, DC0360, DC0510
1	1/2" Hex Head Socket (1/4" drive)	DC0280, DC0360, DC0510
1	Thermally Conductive Compound (Avtron P/N 950010)	ALL
1	#2 Phillips screwdriver	ALL

### 7.8.1 REPLACING THE POWER THYRISTOR (CR1-6), FIELD THYRISTOR (CR7), AND FIELD DIODE (CR8)

#### 7.8.1.1 Disassembly

1. Remove all sources of power from the unit.
2. Remove microprocessor and system boards per section 7.4, steps 1 through 7.
3. Remove bridge interface board per section 7.4, steps 8 through 11.
4. Remove the twisted pairs of wires from gate leads of thyristor to be replaced.

**NOTE**

Each pair of wires is labeled with a single letter corresponding to a letter silkscreened on the base.

5. Refer to Figure 7-9 and Table 7-5. Determine hardware size used to mount bus bar assembly to the thyristors/ diode. Using the torque wrench and the appropriate socket, remove the hardware as shown in Figure 7-9.
6. Remove bus bars from the thyristor.
7. Using the 5/32" Allen wrench socket, remove the mounting screws on each end of the thyristor or diode.
8. Remove the damaged thyristor or diode.

### 7.8.1.2 Replacement and Reassembly

1. Apply a layer of thermally conductive compound to bottom of new thyristor or diode and reinstall in base assembly.
2. Mount new thyristor or diode to heatsink using mounting screws located on each end. Torque tighten the mounting screws to 38-50 in-lb. Recheck torque after a minimum of 3 hours.
3. Replace the bus bars on the thyristor.
4. Replace the hardware mounting the bus bars to thyristor. Torque tighten the screws per the following table.

TABLE 7-6. TORQUE SPECIFICATION

DRIVE SIZE	TORQUE SPECIFICATION	HARDWARE TYPE
FIELD THYRISTOR AND DIODE	22-30 in-lb.	#2 Phillips screw
DC0010, DC0030, DC0056	22-30 in-lb.	#2 Phillips screw
DC0110, DC0180	38-50 in-lb.	#3 Phillips screw
DC0280, DC0360, DC0510	68-75 in-lb.	1/2" hex head bolt

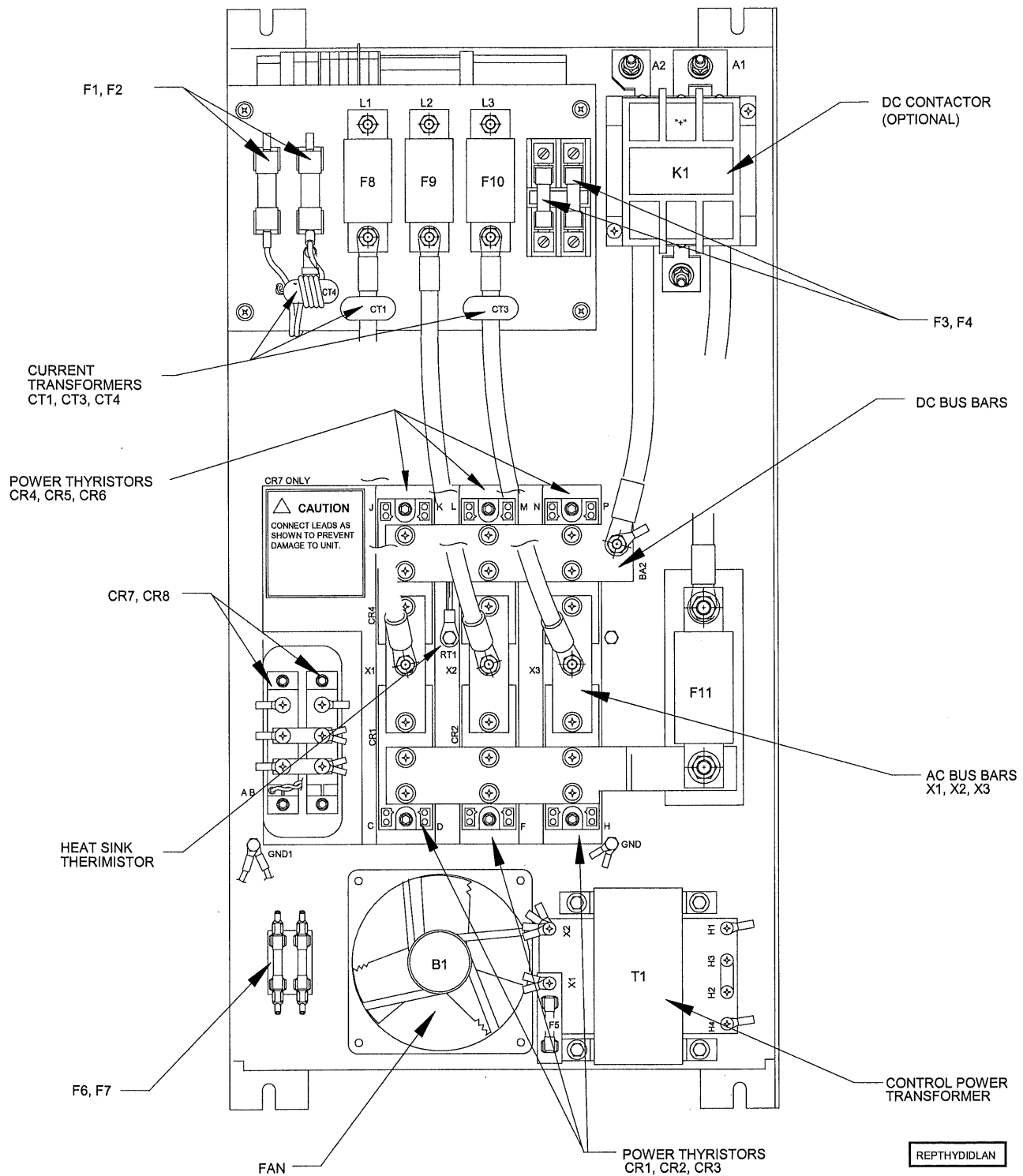


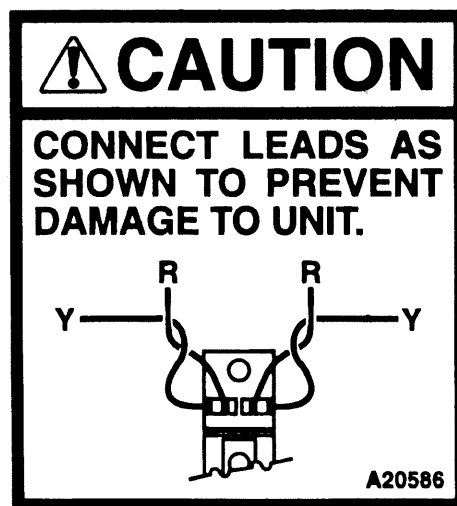
Figure 7-9. Replacing Power Thyristors and Field Thyristor/Diode (510 ADC and Below)

5. Plug in all gate leads. Match letter designation of twisted wire pair to corresponding letter silkscreened on the base.

### NOTE

On thyristors without polarized connector housings, it is important to keep the yellow wire of each pair on "outboard" side of device and the red wire on the "inboard" side.

\*\*\*\*\*



For DC0010 through DC0056 amp sizes, all SCR gate and cathode leads are connected as shown. For DC0110 through DC0510 sizes, only field SCR gate and cathode leads must be connected as shown.

\*\*\*\*\*

6. Slide the bridge interface assembly back on the hinges.
7. Reconnect the J1 cable connection to the snubber assembly and replace the ground wire on the terminal.
8. Attach the two captive screws holding the bridge interface assembly to the base.
9. Slide door assembly onto the hinges.
10. Reconnect the seven cables (J1 thru J7) to the bridge interface board.
11. Replace the ground terminal lug connection on the back of the drive door.
12. Reconnect external system board connections.
13. Verify all connections.
14. Reapply power to the unit.

\*\*\*\*\*

### CAUTION

IT IS NECESSARY TO FOLLOW THE TORQUE SPECIFICATIONS TO INSURE PROPER OPERATION AND RELIABILITY OF THE UNIT.

\*\*\*\*\*

## 7.9 THYRISTOR MODULE AND FUSE REPLACEMENT (550 ADC)

\*\*\*\*\*

### WARNING

HAZARDOUS VOLTAGES WHICH CAN CAUSE SEVERE INJURY OR DEATH ARE PRESENT DURING THE OPERATION OF THIS EQUIPMENT. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE MAKING ANY REPAIRS.

\*\*\*\*\*

1. Remove all sources of power from the unit.
2. Open the main drive door.
3. Refer to Figures 7-3 and 7-6. Remove the bus bar support brace, which is just above the bridge interface assembly, by removing the two quarter-turn fasteners. The three AC fuses (F8-10), the motor armature fuse (F11), and the AC field fuses (F1 and F2) lie behind this brace.
4. Remove the bridge interface assembly, as instructed in section 7.3.4.
5. To replace F8, 9, 10, or 11 fuses, perform the following steps in order:
  - a. Remove the appropriate vertical bus bar.
  - b. Remove the desired fuse with its adjacent bus bars (one at each end) as an assembly. Do this by removing the two 5/16-18 hex head screws that hold the inner adjacent bus bar in place. Use a 1/2" hex head socket wrench.
  - c. Remove the 1/2-13 hex head screws to release the fuse.

- d. Connect the new fuse to the adjacent bus bars using the 1/2-13 screw and 1/2" Belleville springs. Tighten to 335-365 in-lb. Be certain to orient the bus bars properly to each other now, before attaching to the base.
  - e. Reattach the fuse to the base using the two 1/2-13 screws and 5/16" Belleville springs. Tighten to 120-140 in-lb.
  - f. Reattach the vertical bus bar removed in step a.
6. To replace any of the six SCRs CR1-6, perform the following steps in order:
- a. Remove the twisted pairs of wires from the gate leads of the thyristor to be replaced.

**NOTE**

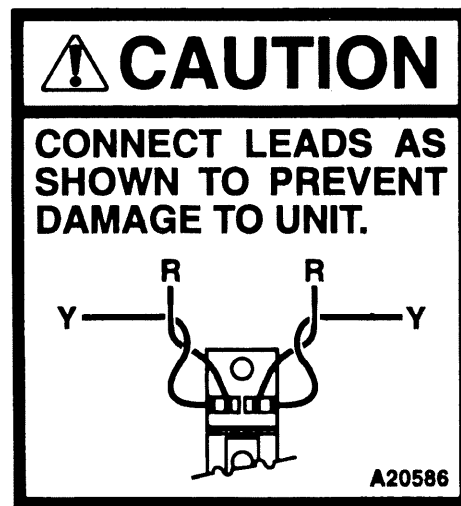
Each pair of wires is labeled with a single letter corresponding to a letter silkscreened on the base.

- b. Remove whatever bus bars are required to gain access to the desired SCR.
  - c. Using a 5/32" Allen wrench, remove the mounting screws on each corner of the thyristor and remove the thyristor.
  - d. Apply a layer of thermally conductive compound to bottom of new thyristor and reinstall. Tighten the #10-24 socket head screws to 38-50 in-lb. Recheck torque after a minimum of 3 hours and apply torque seal.
  - e. Replace the bus bars on the thyristor, using the metric hardware provided with the semiconductor module. Tighten the terminal screws to 70-90 in-lb.
  - f. Reattach the leads removed in step a, being certain to match the letter designations.
7. The field thyristor (CR7) and field diode (CR8) are on the same panel as CR1-6, near the bottom. They may be replaced by the following steps:
- a. Remove the four terminal screws in the thyristor and diode that hold the two bus bars in place, allowing the bus bars to be lifted.
  - b. Remove the terminal screws that attach the remaining wire leads to the device to be replaced.



- c. Using a 5/32" Allen wrench, remove the mounting screws on each end of the device and remove the device.
- d. Apply a layer of thermally conductive compound to bottom of new device and reinstall. Tighten the #10-24 socket head screws to 38-50 in-lb. Recheck torque after a minimum of 3 hours and apply torque seal.
- e. Replace the leads and the bus bars, using the metric hardware provided with the semiconductor device. Tighten the terminal screws to 22-30 in-lb., using a #2 Phillips screwdriver.

\*\*\*\*\*



For 550 ADC models, this **CAUTION** applies to the field SCR (CR7) only. It is important to keep the yellow wire of each pair on the “outboard” side of the device and the red wire on the “inboard” side.

\*\*\*\*\*

8. The control power fuses (F3-7, 12, and 13) are readily accessible just to the right of the field SCR and diode.

**NOTE**

As the unit is shipped, fuses F3 and F4 are 3 amp, for 460/575 VAC operation. To use for 230 VAC input, F3 and F4 must be changed to 5 amp (see Table 7-8b). Fuses to make this change are supplied in a bag attached to the drive. A label is also included which must be affixed to the drive. See paragraph 6.6.4 for reconnection instructions.

9. The AC field fuses, F1 and F2, are located to the right of the motor armature fuse (F11) discussed in step 3. After replacement, F1 hardware should be tightened to 120-140 in-lb. The hardware on F2 should be hand tightened only.
10. Reinstall the bridge interface from step 4 (see paragraph 7.3.4).
11. Attach the bus bar support brace removed in step 3 (two quarter-turn fasteners).
12. Close the main drive door.

## 7.10 THYRISTOR/DIODE/FUSE REPLACEMENT (540, 850, 1550, 3000 ADC) (Refer to Figures 7-11, 7-12, and 7-13.)

\*\*\*\*\*

### WARNING

**HAZARDOUS VOLTAGES WHICH CAN CAUSE SEVERE INJURY OR DEATH ARE PRESENT DURING THE OPERATION OF THIS EQUIPMENT. TURN OFF AND LOCK OUT ALL SOURCES OF POWER BEFORE MAKING ANY REPAIRS.**

\*\*\*\*\*

TABLE 7-7. TOOLS REQUIRED

DESCRIPTION	USED ON ASSEMBLIES
1/4" Drive Torque Wrench (0-75 in-lb.)	Field Supply Subassembly D21591 and D22716
5/32" Hex Head Socket with Allen wrench insert bit (1/4" drive)	Field Supply Subassembly D21591 and D22716
3/8" Drive Torque Wrench (0-500 in-lb.)	DC054X-DC300X Armature Bridge Assembly
9/16" Open End Hex Head Wrench	DC054X-DC085X Armature Bridge Assembly
5/8" Hex Head Socket (3/8" Drive)	DC054X-DC085X Armature Bridge Assembly
Hex Head Socket with #2 Phillips screwdriver insert bit (1/4" drive)	Field Supply Subassembly D21591 and D22716
Thermally Conductive Compound (Avtron P/N 950010)	Field Supply Subassembly D21591 and D22716
#2 Phillips screwdriver	All assemblies
3/4" Open End Hex Head Wrench	DC155X-DC300X Armature Bridge Assembly
3/4" Hex Head Socket 3/8" Drive	DC155X-DC300X Armature Bridge Assembly

7.10.1 REPLACING THE POWER THYRISTOR MODULE ASSEMBLY (A101-106)7.10.1.1 Disassembly

1. Remove power from the drive.
2. Remove the ground lead(s) located in the lower left corner or left center of the back of the drive front panel.
3. Loosen the front panel screws. Using the slotted openings, lift the panel up and off.
4. Unplug cable connector P1 and move the cable away from the module.

**NOTE**

All copper to copper bus work connections are assembled with a thin film of anti-oxidant joint compound (Avtron P/N 905122) between mating surfaces. We recommend using this during reassembly to prevent corrosion at all conductive junctions.

DC0540-DC085X Only (Items 5 through 7 below):

5. Remove the lower bolt holding fuse (F1-6) associated with the module to be replaced to the bus bar. This is located on the left side of modules A101 thru A103 or on the right side of modules A104 thru A106.
6. Remove the bolt attaching the thyristor module assembly to the side bus bar. This is found on the upper right side of modules A101-A103 and on the upper left side of modules A104-A106.

7. Using the fuse (F1-6) as a handle, slowly slide the assembly forward and lift out as a single unit.

\*\*\*\*\*

### W A R N I N G

**THYRISTOR MODULES WEIGH APPROXIMATELY  
25-60 LBS. AND COULD CAUSE PERSONAL INJURY IF  
DROPPED.**

\*\*\*\*\*

#### DC155X-2 and DC155X-4 Only (Items 8a and 9a below):

- 8a. Modules A101-A106: Remove the bolt that holds the top of the fuse to the vertical bus link. Remove the bolt that holds the module to the side bus bar. Using the fuse as a handle, slide the assembly forward and lift out as a single unit.
- 9a. Modules A107-A112: Remove the bolts that attach the module to the bus bars on both the left and right side. Loosen the bolt holding the vertical bus link to the module directly below and rotate the bus link out of the way. Slide the module forward and lift out.

#### DC155X-A and -B Versions, and DC300X (Items 8b and 9b below):

- 8b. Modules A101-A106: If the fuse assemblies are equipped with indicator switches, disconnect the wiring from these first. Remove the bolts that attach both the top and bottom of the fuse assembly bus links to the AC bus bars and thyristor modules. NOTE: Remove the fuses as an assembly, complete with their attached bus work (and indicator switches, if so equipped). Slide the module forward and lift out.
- 9b. Modules A107-A112: Remove the bolts that attach the thyristor module to the bus work on the left and right sides. Slide the module forward and lift out.

7.10.1.2 Reassembly**NOTE**

Conical washers are included in the mounting hardware for thyristor and fuse replacement. Washers must be installed correctly for proper holding pressure. See Figure 7-10.

\*\*\*\*\*

**CAUTION**

**IMPROPER MOUNTING OF CONICAL WASHERS  
COULD RESULT IN DRIVE FAILURE.**

\*\*\*\*\*

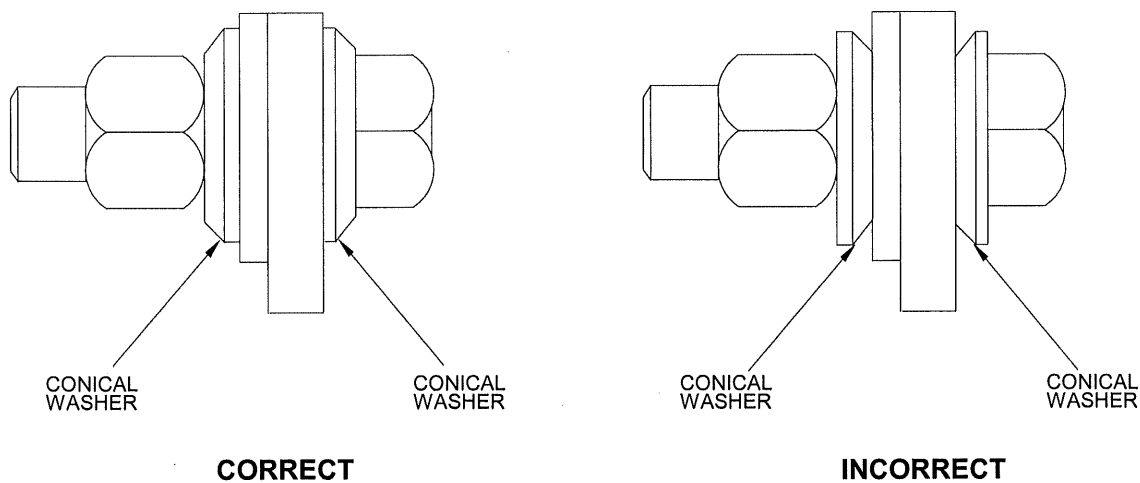


Figure 7-10. Conical Washer Installation

1. Slide new thyristor module into drive.
2. Reverse the disassembly procedure. Use the following table to determine tightening torque for the bolts:

DC54X DC85X	DC155X -2, -4	DC155X -A,-B/DC300X
165-185 in-lb.	335-365 in-lb.	390-420 in-lb.

3. Attach cable connector P1 on all modules.
4. Replace the front panel.
5. Reconnect the ground wire(s) to the front panel.
6. Reapply power to the unit.

\*\*\*\*\*

### CAUTION

**IT IS NECESSARY TO FOLLOW THE TORQUE SPECIFICATIONS TO INSURE PROPER OPERATION AND RELIABILITY OF THE UNIT.**

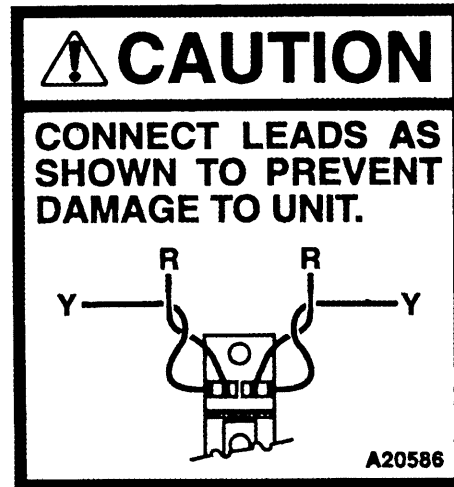
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## 7.10.2 REPLACING THE FIELD THYRISTOR AND DIODE CR1, CR2

### 7.10.2.1 Disassembly

1. Remove power from field supply assembly.
2. Unlatch door of main assembly. (Latches are located on the right side of unit.)
3. Open the door. The bridge interface board (A3) will be exposed.
4. Remove the cables from connectors J2 and J3.
5. Disconnect cable connectors J5 and J6 on the bridge interface board and move the cables out of the way.
6. Loosen the two captive screws holding the bridge interface assembly to the base assembly.
7. Open the bridge interface assembly. The field thyristor (CR1) and field diode (CR2) will be exposed.
8. Unplug the gate leads on the bottom of CR1. Note the connection placement. Twisted pairs of gate lead wires are labeled with a single letter corresponding to a letter silkscreened on the base.

\*\*\*\*\*



For DC0010 through DC0056 drive sizes, all SCR gate and cathode leads must be connected as shown. For DC0110 and larger drive sizes, only field SCR gate and cathode leads must be connected as shown.

\*\*\*\*\*

9. Remove the three Phillips head screws on CR1 and CR2 (six total). Note connection placement.
10. Move the two bus bar links away from the thyristor and diode.
11. Remove the screws on each end of the device (CR1 or CR2) to be replaced.

#### 7.10.2.2 Replacement and Reassembly

1. Apply a thin layer of thermally conductive compound to the bottom of new thyristor or diode and reinsert in the field supply base.
2. Mount the new thyristor or diode using the screws located on each end. Torque tighten the mounting screws to 38-50 in-lb. Recheck torque after a minimum of 3 hours.
3. Reinstall the wiring, bus bar connections and mounting hardware. Torque tighten the screws to 22-30 in-lbs.
4. Plug in gate leads on CR1, observing correct polarity. The yellow leads should face the "outboard" side of the device; the red leads should face the "inboard" side.
5. Tighten the two captive screws holding the bridge interface assembly to the base.
6. Plug in connectors J5 and J6 to the bridge interface board (A3).



7. Plug in cables at J2 and J3.
8. Close the door of the field supply assembly and reapply power.

\*\*\*\*\*

**CAUTION**

**IT IS NECESSARY TO FOLLOW THE TORQUE  
SPECIFICATIONS TO INSURE PROPER OPERATION  
AND RELIABILITY OF THE UNIT.**

\*\*\*\*\*

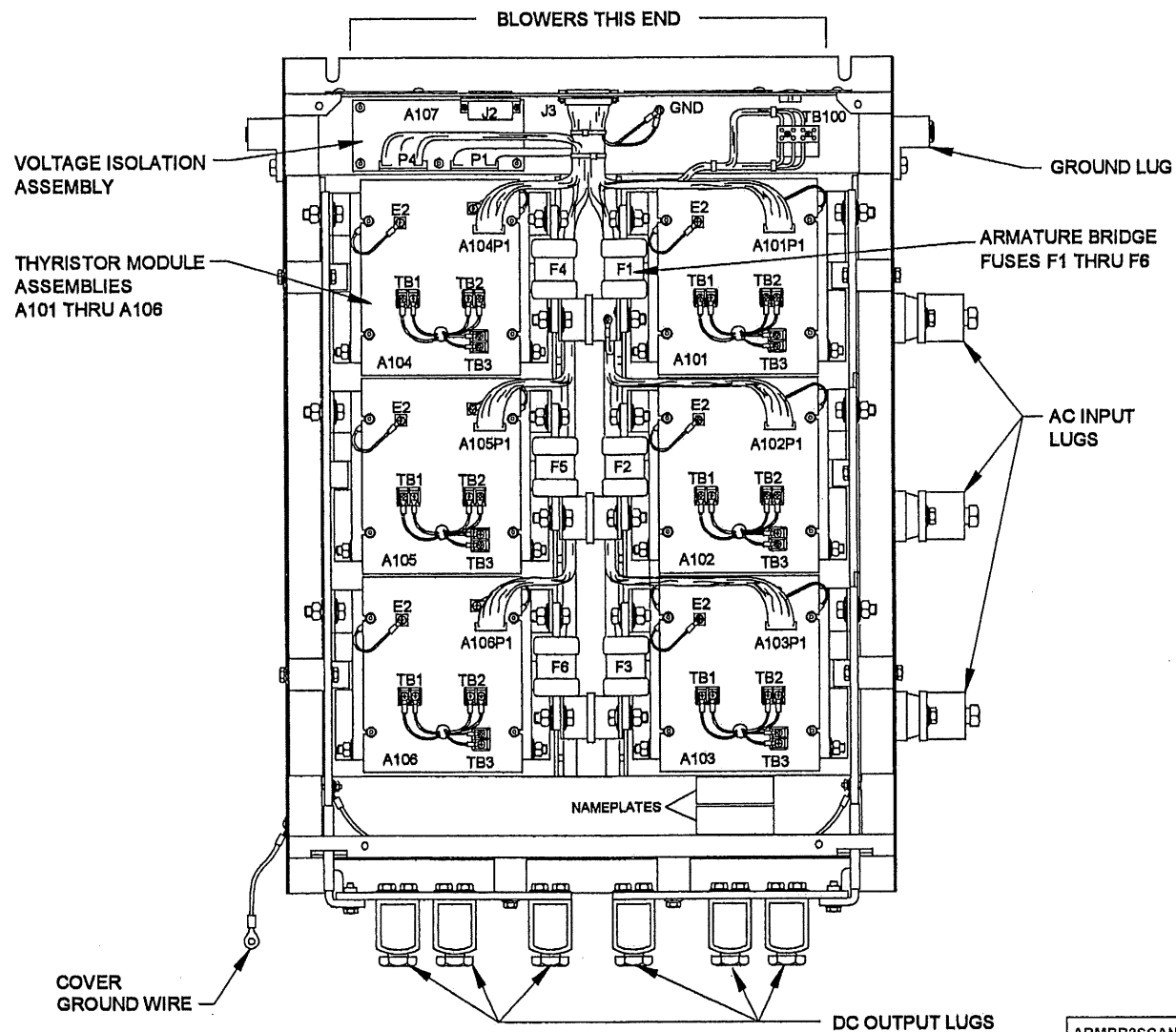


Figure 7-11. Armature Bridge Assembly (540 and 850 Amp)

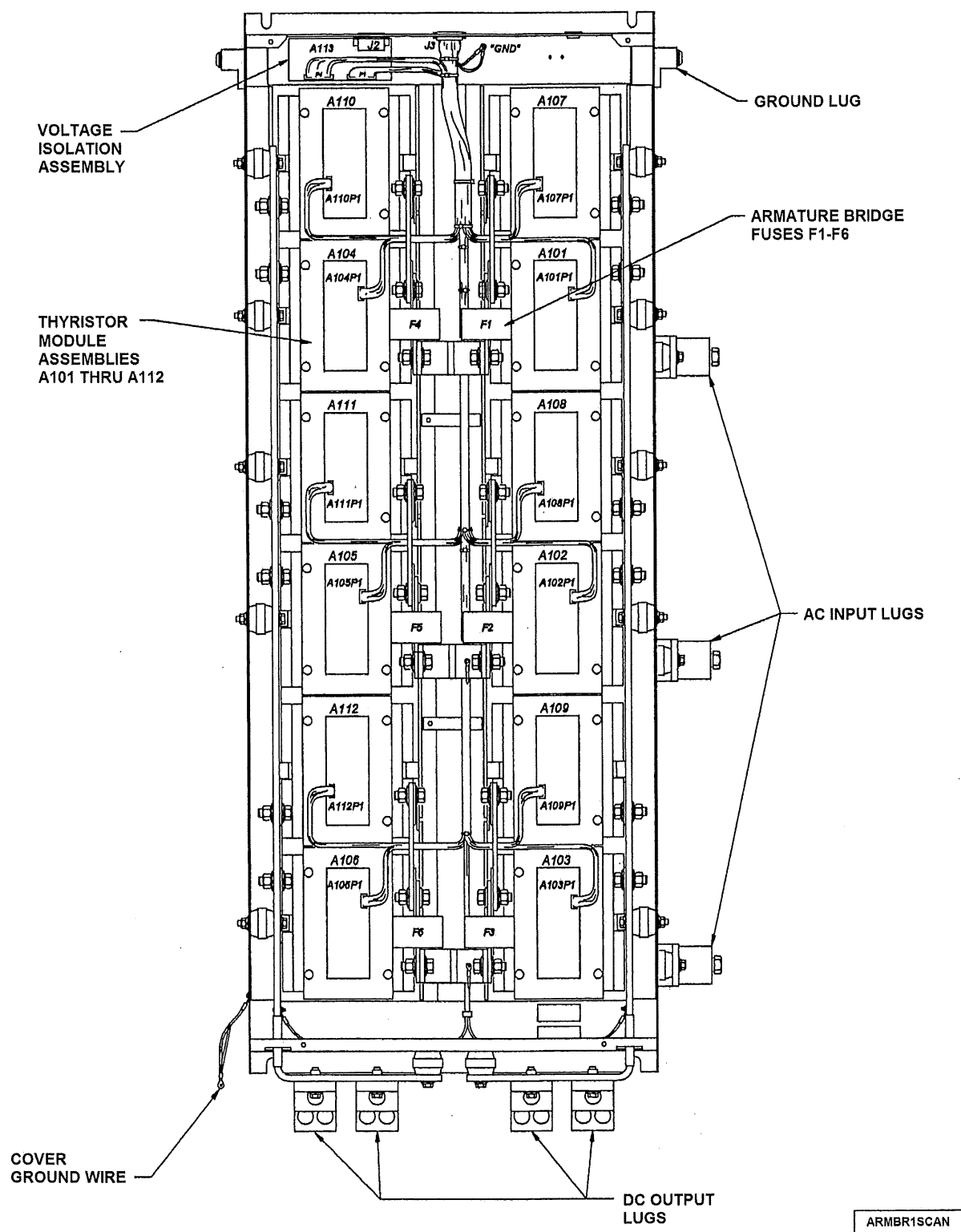


Figure 7-12. Armature Bridge Assembly 155x-2 or -4 Only

NOTE: Fuses F1 through F6 are parallel fuse units on DC250X units.

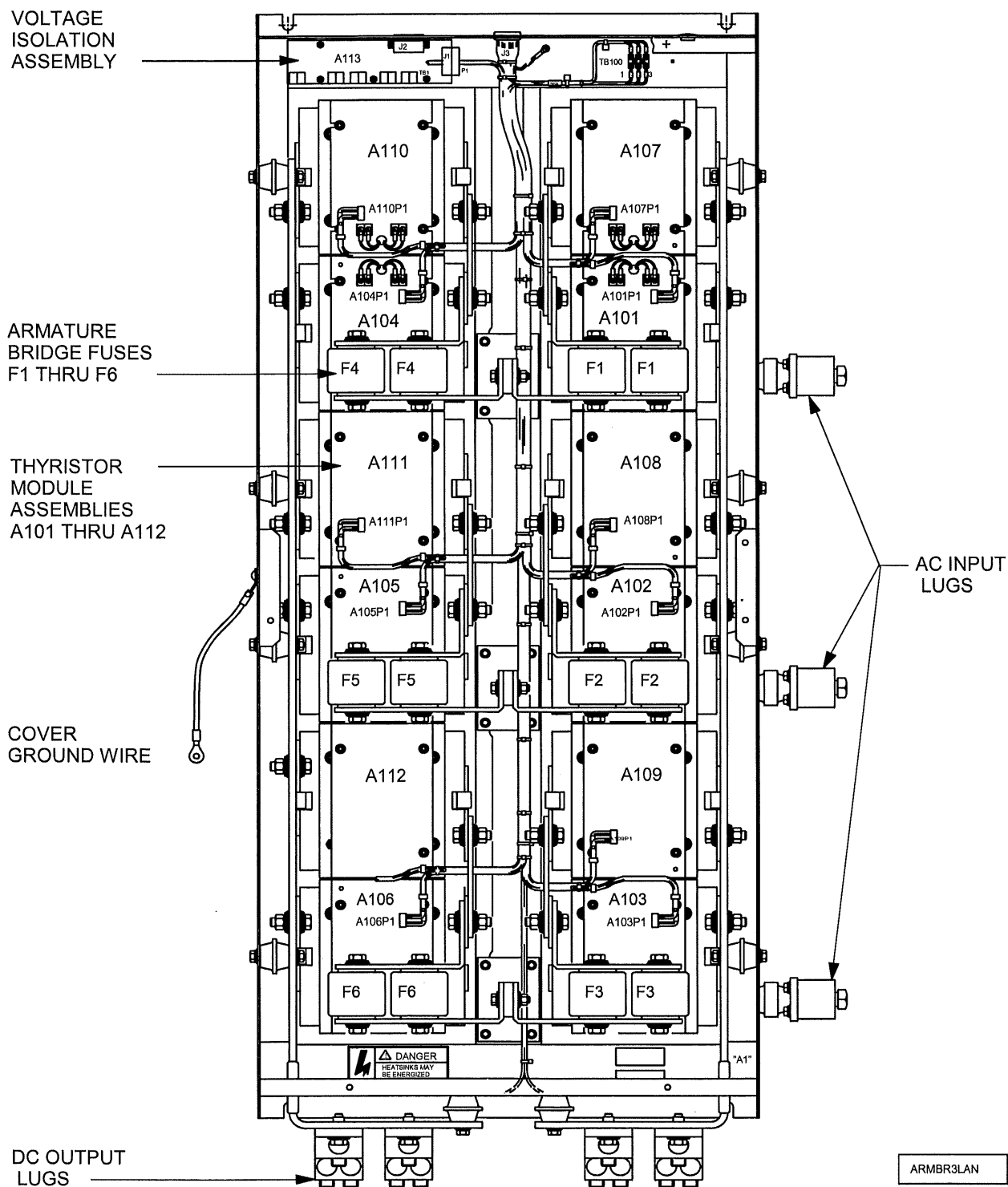


Figure 7-13. Armature Bridge Assembly (155X-A &amp; -B and 300X)

TABLE 7-8a. FUSE REPLACEMENT GUIDE (10-510 ADC)

(Refer to Figure 7-5 for fuse location.)

DRIVE RATING (AMPS)	F1,F2 RATING/ P/N	F3,F4 RATING/ P/N	F5 RATING/ P/N	F6 RATING/ P/N	F7 RATING/ P/N	F8,F9,F10 RATING/ P/N	F11 RATING/ P/N
10	5A, 500V/ 324438	2A, 600V/ 324452	3A, 250V/ 324451	1A, 250V/ 324195	0.6A, 250V/ 324008	40A, 500V/ 324442	50A, 700V/ 324441
30	5A, 500V/ 324438	2A, 600V/ 324452	3A, 250V/ 324451	1A, 250V/ 324195	0.6A, 250V/ 324008	40A, 500V/ 324442	50A, 700V/ 324441
56	10A, 500V/ 324439	2A, 600V/ 324452	3A, 250V/ 324451	1A, 250V/ 324195	0.6A, 250V/ 324008	60A, 500V/ 324444	80A, 700V/ 324443
110	10A, 500V/ 324439	3A, 600V/ 324453	5A, 250V/ 324184	1A, 250V/ 324195	1.25A, 250V/ 324019	175A, 500V/ 324455	200A, 700V/ 324459
180	20A, 500V/ 324440	4A, 600V/ 324454	5A, 250V/ 324184	1A, 250V/ 324195	1.25A, 250V/ 324019	300A, 500V/ 324456	300A, 700V/ 324447
280	20A, 500V/ 324440	5A, 600V/ 324475	6.25A, 250V/ 324154	1A, 250V/ 324195	1.25A, 250V/ 324019	400A, 500V/ 324457	400A, 700V/ 324460
360	20A, 500V/ 324440	5A, 600V/ 324475	6.25A, 250V/ 324154	1A, 250V/ 324195	1.25A, 250V/ 324019	500A, 500V/ 324458	500A, 700V/ 324461
510	20A, 500V/ 324440	5A, 600V/ 324475	6.25A, 250V/ 324154	1A, 250V/ 324195	1.25A, 250V/ 324019	600A, 500V/ 324492	700A, 700V/ 324704

\*\*\*\*\*

**WARNING**

**REPLACE FUSES WITH FUSE OF SAME TYPE AND RATING. IMPROPER FUSE REPLACEMENT MAY RESULT IN DAMAGE TO THE ADDvantage-32, A FIRE HAZARD, AND SEVERE INJURY OR DEATH TO PERSONNEL.**

\*\*\*\*\*

TABLE 7-8b. FUSE REPLACEMENT GUIDE (550 ADC)

DRIVE RATING	F1,F2 RATING/ P/N	F3,F4 RATING/ P/N*	F5 RATING/ P/N	F6 RATING/ P/N	F7 RATING/ P/N	F8,F9,F10 RATING/ P/N	F11 RATING/ P/N	F12 RATING/ P/N	F13 RATING/ P/N
550 ADC Armature, 12 ADC Field	60A, 700V 324730	*	8A, 250 VAC/ 324199	1A, 250 VAC/ 324195	1.25A, 250 VAC/ 324397	630A, 700V/ 324808	700A, 1200V/ 324807	3A, 250V/ 324451	3A, 250V/ 324451
550 ADC Armature, 24 ADC Field	60A, 700V 324730	*	8A, 250 VAC/ 324199	1A, 250 VAC/ 324195	1.25A, 250 VAC/ 324397	630A, 700V/ 324808	700A, 1200V/ 324807	3A, 250V/ 324451	3A, 250V/ 324451
550 ADC Armature, 48 ADC Field	60A, 700V 324730	*	8A, 250 VAC/ 324199	1A, 250 VAC/ 324195	1.25A, 250 VAC/ 324397	630A, 700V/ 324808	700A, 1200V/ 324807	3A, 250V/ 324451	3A, 250V/ 324451

\*If unit is operated at 230 VAC input, F3 and F4 are 5A, 600V Class CC, P/N 324475.

If unit is operated at 460/575 VAC input, F3 and F4 are 3A, 600V, Class CC, P/N 324453.

See Section 6.6.2 for configuration instructions.

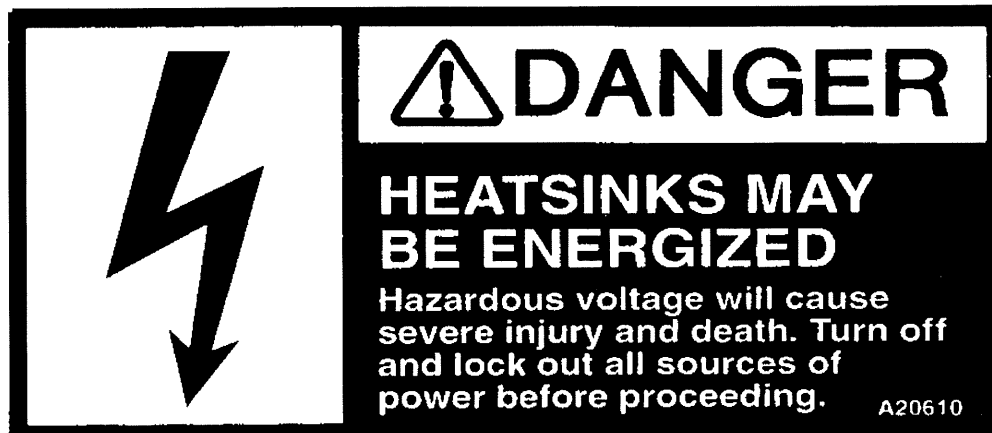
TABLE 7-9. VENDOR GUIDE

AVTRON P/N	FUSE RATING	BUSSMANN P/N	LITTELFUSE P/N	GOULD P/N	FERRAZ P/N
324008	0.6A, 250V	MDL-1.6			
324019	1.25A, 250V	MDL-1.25	313-1.25		
324154	6.25A, 250V	MDA-6.25	326-6.25		
324184	5A, 250V	MDA-5	326-5		
324195	1A, 250V	MDA-1	326-1		
324199	8A, 250V	MDA-8	326-8		
324267	1400A, 700V				A070URD33TTI1400
324397	1.25A, 250V	MDA-1.25	326-1.25		
324438	5A, 500V	FWH-5			A050F005
324439	10A, 500V	FWH-10	L50S-10	A50P10	A050F010
324440	20A, 500V	FWH-20	L50S-20	A50P20	A050F020
324441	50A, 700V	FWP-50A	L70S-50	A70P50	A070F050
324442	40A, 500V	FWH-40A	L50S-40	A50P40	A050F020
324443	80A, 700V	FWP-80A	L70S-80	A70P80	A070F080
324444	60A, 500V	FWH-60A	L50S-60	A50P60	A050F060
324447	300A, 700V	FWP-300A		A70P300	A070F300
324451	3A, 250V	MDA-3	326-3		
324452	2A, 600V	FNQR-2	KLDR-2		
324453	3A, 600V	FNQR-3	KLDR-3		
324454	4A, 600V	FNQR-4	KLDR-4		
324455	175A, 500V	FWH-175A	L50S-175	A50P175	A050F175
324456	300A, 500V	FWH-300A	L50S-300	A50P300	A050F300
324457	400A, 500V	FWH-400A	L50S-400	A50P400	A050F400
324458	500A, 500V	FWH-500A	L50S-500	A50P500	A050F500
324459	200A, 700V	FWP-200A		A70P200	A070F200
324460	400A, 700V	FWP-400A		A70P400	A070F400
324461	500A, 700V	FWP-500A		A70P500	A070F500
324475	5A, 600V	FNQR-5	KLDR-5		
324492	600A, 500V	FWH-600A	A050F600	A50P600	XL50F600
324776	1400A, 700V				A070URD33LI1400
324783	2000A, 1000V				A100URB20002PFBI
324802	700A, 700V				A070URD33TTI0700
324803	700A, 1300V				A130URD73TTI0700
324806	900A, 1300V				A130URD73TTI0900
324807	700A, 1200V				D075RB700K3B1
324808	630A, 700V				A070URD33THI0630

## 7.11 FUSE REPLACEMENT (540, 850, 1550, 3000 ADC)

### 7.11.1 FUSE REPLACEMENT FOR ARMATURE BRIDGE ASSEMBLY

#### 7.11.1.1 Disassembly



1. Remove power from the drive.
2. Disconnect the ground wire(s) located on the lower left corner or left/center on the back of the front panel.
3. Loosen the front panel screws. Using the slotted openings, lift the panel up and off.
- 4a. DC054X, DC085X, and DC155X-2 and -4 versions only:  
Remove the two bolts holding the fuse to be replaced (F1-F6) between the bus bars and thyristor module.
- 4b. DC155X-A and -B, DC250X, and DC300X:  
Remove the wires from the fuse indicator switch, if so equipped. Remove the mounting bolts that attach the fuse bus links to the AC bus bars and the thyristor module. NOTE: The fuses, indicator switches, and associated bus links should be removed as an assembly. Once removed, the bus links can be detached from the fuses. If replacing a fuse that is equipped with an indicator switch, remove the two screws that attach the switch to the fuse.



### 7.11.1.2 Replacement and Reassembly

1. Refer to Figure 7-9 for proper hardware installation.
2. Install the new fuse(s) and torque tighten the bolts per the following table:

DC054X, DC085X	DC155X-2 and -4	DC155X-A and -B DC300X
165-185 In-lb.	335-365 In-lb.	(Bus Link to Bus Bar) 390-420 In-lb. NOTE: The 1/2" bolts that attach the bus links to the fuse ends should be torque tightened to 335-365 In-lb.

3. Replace the front panel.
4. Reconnect the ground wire(s) to the front cover.
5. Reapply power.

## 7.11.2 FUSE REPLACEMENT - FIELD SUPPLY ASSEMBLY

### 7.11.2.1 Disassembly

1. Remove power from the field supply assembly.
2. Unlatch door of main assembly. (Latches are located on the right side of unit.)
3. Open the door. Bridge interface board (A3) will be exposed.
4. Remove cables from connectors J2 and J3.
5. Disconnect cable connectors J5 and J6 on bridge interface board and move cables aside.
6. Open bridge interface assembly to expose the fuses.

### 7.11.2.2 Replacement and Reassembly

1. Fuses F3 and F4 are removed by removing the nuts from the studs to which the fuses are mounted. The remainder of the fuses can be removed manually or by using a screwdriver.
2. Install new fuse and tighten the nuts on the studs if necessary.
3. Tighten two captive screws holding bridge interface assembly to the base.
4. Plug connectors J5 and J6 onto bridge interface board (A3).
5. Plug cables into J2 and J3.
6. Close door of field supply assembly and reapply power.

TABLE 7-10. FUSE REPLACEMENT GUIDE

(Applies to Amp Ratings DC054X, DC085X, DC155X, DC300X)

ASSEMBLY/ REF. DES.	RATING/ AVTRON P/N	BUSSMANN P/N	GOULD P/N	FERRAZ P/N	LITTELFUSE P/N
Field Supply/ F5	1A, 250V/ 324195	MDA-1	--	--	326-1
Field Supply/ F3,F4	60A, 500V/ 324444	FWH60A	A50P60	A050F060	L50S-60
Field Supply/ F1,F2,F6,F7,F8	*				
DC0540-DC085X Armature Bridge/ F1-6	600A, 500V/ 324492	FWH600A	A50P600	A050F600	L50S-600
DC155X-2 and -4 Armature Bridge/ F1-F6	1400A, 700V/ 324776			A070URD- 33LI1400	
DC155X-A	700A, 700V/ 324802				
DC155X-B	700A, 1300V/ 324803				
DC300X-A	1400A, 700V/ 324267				
DC300X-B	900A, 1300V/ 324806				

\* Application specific fuses. Refer to applicable system drawings for current ratings of application specific fuses. F1 and F2 must be 500V Class CC fuses rated at a maximum of 25A. F6 must be rated at 5A or less, 250V minimum. F7 must be rated at 12A or less, 120V minimum. F8 must be rated at 20A or less, 120V minimum.

**7.12      THYRISTOR MODULE COOLING BLOWER REPLACEMENT (550 ADC)**

1. Remove power from the unit.
2. Open main drive door.
3. Refer to Figure 7-3. Remove the panel with the circular grill by removing eight Phillips-head screws. The inlet ring is also attached to this panel.
4. With a long nut driver, remove the four #10-24 self-locking nuts that hold the blower support and blower to the base.
5. With the blower partially removed, reach under the chassis and disconnect the power cable connector from J100. The blower can now be removed.
6. Separate the blower support from the blower by removing four M6x12 screws.
7. Reverse the above steps to install the new blower.



## **SECTION VIII**

# **IEEE 802.3 ETHERNET COMMUNICATION**

### **8.1 OVERVIEW**

The Avtron ADDvantage-32 DC and AC Drives support an 802.3 Ethernet star structured network. The ADDvantage-32 supports both 100 base FX Fiber Optic and 10/100 base UTP Copper Ethernet media. The Avtron Ethernet network is implemented using an Avtron ESBX Ethernet board, P/N A26494 that can provide 100 Mbaud fiber full duplex IEEE 802.3 Ethernet communications. One ESBX board is required for each ADDvantage-32 drive. The ESBX board includes firmware to implement Ethernet protocols for GE, Modicon, and Rockwell PLC interfaces. In addition, the firmware includes Avtron's proprietary communications protocol, Peer Primitive. The Peer Primitive protocol enables Autoscan/Exchange communications among ADD-32 drives and provides the backbone for high speed communications to Avtron's Performance View Graphic Trending / Historical Event Recorder and Avtron's ADDAPT 2000 drive maintenance tool. The ESBX board can communicate using up to four different Ethernet protocols simultaneously over the same network cable which provides great flexibility in system design.

A managed high speed Ethernet Switch is usually provided with Avtron's Ethernet based drive systems. The Avtron provided Switch may include multiple 100 Mbaud fiber ports and multiple 10/100 Mbaud copper ports. The managed Ethernet Switch is the central node of the network and will guarantee deterministic communication to all nodes by providing one full duplex 802.3 communication port for each device on the network. Full duplex operation of a single device per port assures no data collisions can occur. Many of the provided Switches have built in Switch diagnostic functions. These diagnostics greatly enhance network maintenance capability by providing independent diagnostics for each port which can quickly identify and localize a network problem.

Patch/Wic boxes may have been provided to manage excess fiber cable and provide a means to connect each drive to the multi conductor field installed cable by way of an easily replaceable fiber patch cord cable. In the event a fiber patch cable connected to an ADD-32 drive is damaged, it is easy and inexpensive to replace the patch cable leaving the permanently installed fiber cable undisturbed.

Avtron PDC-6 drive control systems using 802.3 Ethernet communications provide a high level of reliability, performance, and diagnostics. Utilization of the 802.3 Ethernet requires ADDvantage-32 hardware and firmware capable of Ethernet support.

### 8.1.1 ESBX Ethernet Board

The ESBX Ethernet board P/N A26494 Rev. D and higher is hardware configurable to use either Fiber Optic or Twisted Pair UTP (Copper) media. This board is shipped from Avtron configured for use with fiber optic media. To reconfigure ESBX board for twisted pair (copper) media, move jumpers TP2 and TP3 on board from positions 1 and 2 to positions 2 and 3.

The ESBX Ethernet board P/N A26494 Rev. C and lower is pre-assembled to use fiber optic media and cannot be modified to use copper. The RJ45 connector exists on this fiber version simply for manufacturing simplicity. ESBX Ethernet board P/N A26495 is pre-assembled to use twisted pair (Copper) media and cannot be modified to use fiber. This copper ESBX board P/N A26495 has now been replaced with P/N A26494 Rev. D and higher.

P/N A26494 Rev D and higher = Fiber Optic or Twisted Pair UTP Copper Media

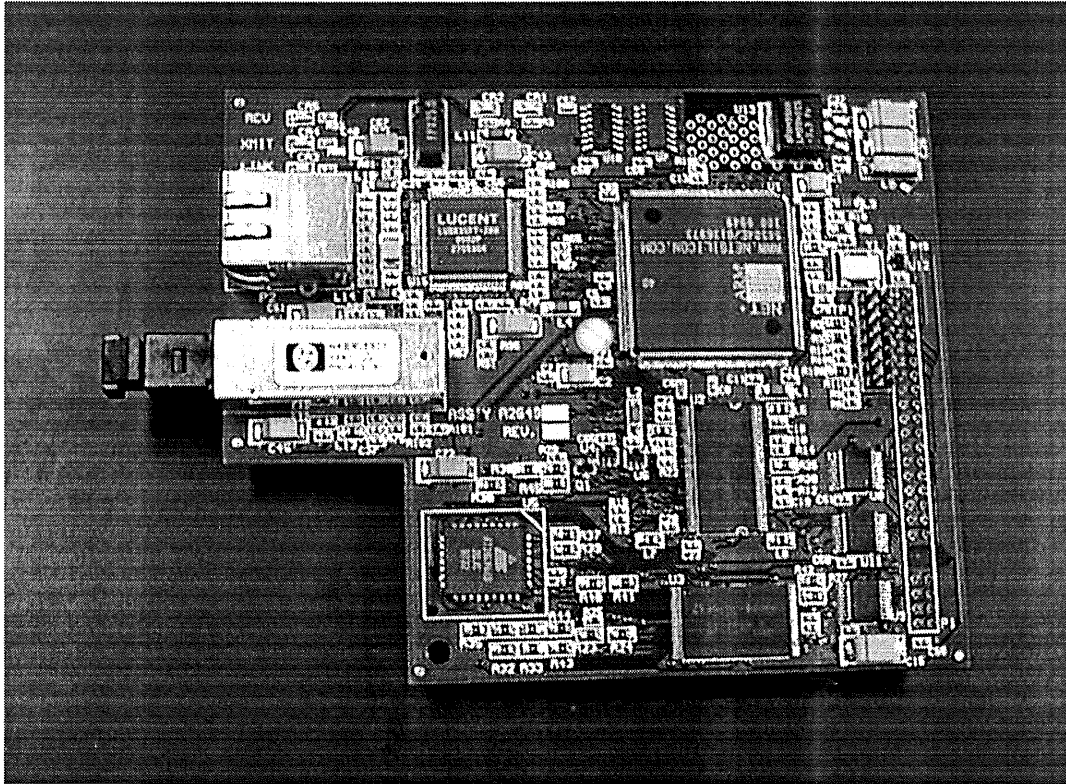
P/N A26494 Rev C and lower = Fiber Optic Media Only

P/N A26495 = Twisted Pair UTP Copper Media Only (Superseded by P/N A26494 Rev D and higher)

ESBX Physical Ethernet interface: 100 MHz Fiber, full duplex, MTRJ connector

10/100 Meg Copper UTP, half/full duplex,  
RJ-45 connector

Each ESBX board has been assigned a unique MAC Address. The MAC Address is printed on a label located on the component side of the ESBX board. The MAC Address has also been programmed into ESBX firmware by Avtron.



**Figure 8-1. Avtron ESBX Module**

The ESBX boards are sensitive to Electro Static Discharge (ESD). These boards must be properly handled using an Anti-Static Wrist Wrap connected to a good ground! The ESBX boards must be carried and/or shipped in approved Anti Static bags!

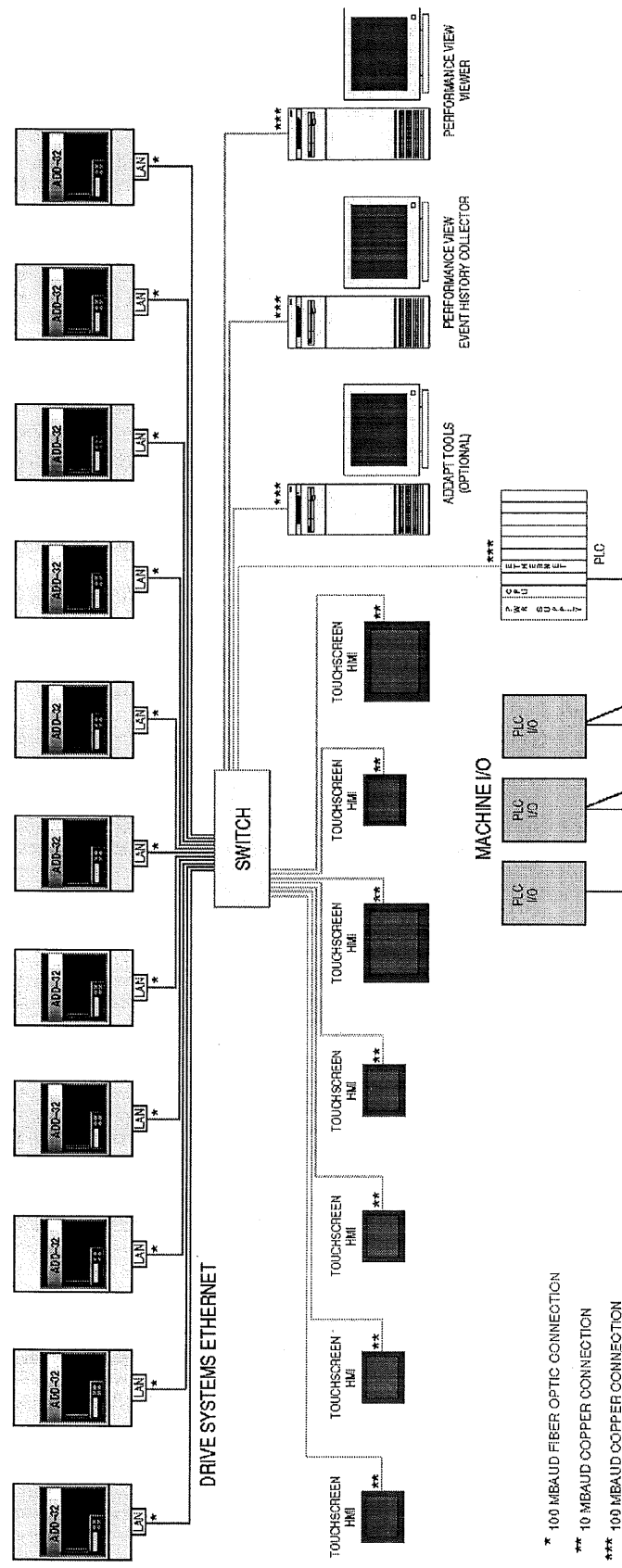
One ESBX Ethernet board is required for each ADDvantage-32 Drive. The ESBX board plugs into SBX connector J4 on the System Maxi board for ADDvantage-32 DC Drives and SBX connector J11 on the Microprocessor board for ADDvantage-32 AC Drives. Install the ESBX board by inserting board connector into the SBX connector. Make sure that both the top and bottom of the ESBX board are fully inserted. Screw down the ESBX board using nylon screw.

The ESBX board has five LED's in the upper left corner for visual indication of board operation. The LED's are defined as:

CR1 LED:	Normally flashing amber about once per second. This LED indicates communication between the drive and the ESBX board.
CR2 LED:	Normally off. This LED is controlled by the processor and is for Avtron debug use only.
RCV LED:	Green flash during receive of incoming frame data.
TX LED:	Green flash during transmitting of outgoing frame data.
Link Active LED:	Illuminates solid Red after 30 second boot up following drive power cycle or drive reset, provided there is a valid cable connection to an Ethernet Switch or device.

The following picture shows an overview of a typical Avtron Drive System utilizing Ethernet communications.





\* 100 MBAUD FIBER OPTIC CONNECTION  
\*\* 10 MBAUD COPPER CONNECTION  
\*\*\* 100 MBAUD COPPER CONNECTION

## 8.2 ADDvantage-32 HARDWARE/SOFTWARE REQUIREMENTS

Most ADDvantage-32 drives manufactured after mid 1994 can be easily field upgraded for Ethernet support without requiring any drive board replacements. Avtron service engineers have routinely upgraded many systems during normally scheduled maintenance outages of 8 to 12 hours. If drives have previously used 802.4 LAN communications, installation of the ESBX Ethernet board requires removal of the 802.4 Modem (P/N A22122) on the Maxi System board.

The ADDvantage-32 boards can be identified by a part number and revision level which is ink stamped on the component side of the board. An existing drive can be field upgraded for Ethernet support if the drive currently uses 692xxx application software and has a MAXI System Board with a part number of A18876-1 or A19359-1. All Bridge Interface Boards (BIB) that are in drives running 691xxx application software (or later) will support Ethernet. Very old Bridge Interface Boards, typically the non "-1"s, will not support Retentive Setpoints, which is the real compatibility issue, not Ethernet.

The following represents the hardware and software requirements for Ethernet Support:

### Hardware Requirements

- High Memory Microprocessor Board P/N 630264 with Boot PROM (U9) software P/N 680635 V15 or higher.
- MAXI System Board must be P/N A18876-1 or A19359-1.
- Maxi System Board requires serial EPROM (U5) software P/N 681444.V11 or greater (sometimes labeled as 444).
- Removal of Modem Board P/N A22122 if 802.4 LAN communications has been previously used.
- ESBX Ethernet Board P/N A26494 (Rev. D and higher) - Hardware configurable for Fiber Optic or UTP Copper twisted pair media.
- Compatible Managed Ethernet Switch for network.
- Fiber Optic Cables and/or CAT 5 Cables.

## **Software Requirements**

- ADDvantage-32 Application Software P/N 694xxx for DC Drives or P/N 695xxx for AC Drives.
- ADDAPT 2000 must be used if the ADDvantage-32 Application Programming Tools are required. ADDAPT Dos and ADDAPT 98 do not support Ethernet communication.
- Performance View System must be used if Historical trending and logging of I/O events is required as the DOS version of Event History Recorder does not support Ethernet.

## **8.3 ADDvantage-32 DRIVE ID/IP ADDRESS AND CONFIGURATION**

### **8.3.1 DRIVE ID/IP Address**

The ADDvantage-32 Drive ID is set by binary weighted inputs from hard-wired jumpers on the Maxi System Board J8 connector for DC Drives and the J6 connector on Microprocessor board for AC Drives. This is the only place you can confirm that the terminal blocks are wired as required to give you the desired Drive ID. The Drive's ID applies to the RS-485 Serial Link, 802.4 Local Area Network (LAN) and possibly to 802.3 Ethernet.

The ADDvantage-32 drive also has an Ethernet IP address which is relevant when the drive has an ESBX Ethernet board installed and running application software P/N 694xxx or 695xxx. The Ethernet IP address contains four numeric fields called "Octets" that are separated by a decimal point between fields. An Octet is a numerical value made up of eight binary places (bits). Octets can represent decimal numbers from zero (0000 0000) to 255 (1111 1111). Each of the four fields can contain a number ranging from 0 to 255. An example IP address is 10.1.206.6 (referred to as, " ten point one point two zero six point six).

The Ethernet IP address can be assigned to the ADDvantage-32 drive by either the "HARD SET" or "DRIVE ID BASED" method.

The "HARD SET" IP address method has all four fields of the IP address set by drive calibration parameters in the "DRIVE CALIBRATE" menu. The four calibration parameters that define the IP Address are "IP ADDR HI", "IP ADDR HM", "IP ADDR LM" and "IP ADDR LO". Note that IP ADDR LO must not be set to 256 for the "HARD SET" method. Be aware that if the "HARD SET" IP method is used, the DRIVE ID is still required for ADDAPT 2000 operation.

The "DRIVE ID" BASED address method is the same as the HARD SET IP, with the following exception: IP ADDR LO must be set to 256. The drive will then use the DRIVE ID as set by the hard wired jumpers for the number in the lowest octet field of the IP ADDRESS. The reason for the DRIVE ID BASED address is to allow the drive to have a default ETHERNET IP address that will allow ETHERNET communications from an initial power up

without any edit of drive cal data. The default IP ADDRESS for any drive is: 10.1.206.LAN ID. The ADDvantage-32 Drive reads the DRIVE ID jumper configuration on power up and displays the DRIVE ID as "DRIVE COM ID" in the "DIAGNOSTICS" menu. Changes to the DRIVE ID jumpers require a drive reset or power cycle before the new DRIVE ID takes effect.

An example of a DRIVE ID BASED address:

DRIVE ID = 12

IP ADDR HI = 10

IP ADDR HM = 1

IP ADDR LM = 206

IP ADDR LO = 256

This would result in an actual drive IP ADDRESS = 10.1.206.12

### 8.3.2 ADDvantage-32 DRIVE ETHERNET CONFIGURATION

Only ADDvantage-32 Application software P/N 694xxx (DC Drive) and P/N 695xxx (AC Drive) support Ethernet. A valid IP Address, Subnet Mask (MSK), and Gateway (GWY) Address must be entered for their respective "X" parameters in the "Drive Calibrate" menu. These numbers will be the same for all drives in a system except for the last octet (LO address) of the IP Address (if the 256 DRIVE ID address method is used, they can all match). It will be necessary to manually set the IP Address, Subnet Mask, Default Gateway and Machine NO parameters of a spare drive or Microprocessor board that is installed to replace a failed drive. Until these parameters are correctly set for the replacement drive, the drive will not communicate correctly over ETHERNET. You will not be able to download Calibration and Configuration data to the drive via ADDAPT 2000 over ETHERNET until these parameters are correctly set.

Obtain unused IP addresses from your MIS or IT department when setting up drives on a network so the ID jumper may be set accordingly (or set ADDR LO to the available last octet). If you are unsure if an IP Address is already used, use the "PING" command at a DOS prompt on a PC connected on the network. The "PING" command can be used to test the communication between two programs over the network. To invoke the PING command, go to a Dos prompt and type "ping xxx.xxx.xxx.yyy", where xxx.xxx.xxx is the 1<sup>st</sup> three octets of the other device's IP address and yyy is the number you picked. If you receive *Request Timeouts*, there is nothing currently on the network using that address. However, if the drives are connected to your company's network, and you don't obtain an address from your MIS Department, there could be a device that is currently off that could be turned on at a later time resulting in problems. The following illustrates a return following a PING command:

C:\>ping 10.1.207.213

Pinging 10 1.207.213 with 32 bytes of data:

Reply from 10.1.207.213: bytes=32 time<10ms TTL=128

Reply from 10.1.207.213: bytes=32 time<10ms TTL=128

Reply from 10.1.207.213: bytes=32 time<10ms TTL=128

Reply from 10.1.207.213: bytes=32 time<10ms TTL=128

Ping statistics for 10.1.207.213:

Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),

Approximate round trip times in milli-seconds:

Minimum = 0ms, Maximum = 0ms, Average = 0ms

“Request timed out” indicates the device is not present or not communicating.

“Destination host unreachable” indicates you are not on the correct network or are not connected.

There are ESBX Ethernet configuration parameters contained in “DRIVE CALIBRATE”(X) and “DRIVE CONFIGURE” (Y) menus of the ADDvantage-32 Drive. The parameter numbers will vary depending on the ADDvantage-32 Application software being used and will be noted below as “\*\*\*”. Please reference Appendix C of your ADDvantage-32 Drive manual that shows the parameter listing for your application software.

### **Drive Calibrate Menu – “X” Parameters**

#### **DRIVE IP ADDRESS:**

X\*\*\*: IP ADDR HI: Highest octet of the DRIVE IP ADDRESS. Range 1-255, default = 10

X\*\*\*: IP ADDR HM: High Middle octet of the DRIVE IP ADDRESS. Range 1-255, default = 1

X\*\*\*: IP ADDR LM: Low Middle octet of the DRIVE IP ADDRESS. Range 1-255, default = 206

X\*\*\*: IP ADDR LO: Low octet of the DRIVE IP ADDRESS. Range 1-256, default = 256

Each ADDvantage-32 drive on the network must have a unique IP address assigned via X090-X093 parameters. Parameter X093 may be set to a special value of “256” that indicates the LOW OCTET of the IP address should be set to the DRIVE ID ADDRESS. The ADDvantage-32 drive IP address may need to be changed from default values to meet your specific company’s requirements. If not specified by your MIS or IT Department, the IP address can be left at the default values. Be aware that duplicate IP Addresses on the network will cause communication problems and failures!

**DRIVE SUBNET MASK:**

X***: MSK ADDR HI:	Highest octet of the DRIVE SUBNET MASK – range 0-255, default = 255
X***: MSK ADDR HM:	High Middle octet of DRIVE SUBNET MASK – range 0-255, default = 255
X***: MSK ADDR LM:	Low Middle octet of DRIVE SUBNET MASK – range 0-255, default = 0
X***: MSK ADDR LO:	Lowest octet of the DRIVE SUBNET MASK – range 0-255, default = 0

The Drive Subnet Mask is defaulted to a value that will allow operation on the Avtron Cleveland Network. The values of the Subnet Mask may need altered to match the specifics of your company's network. Your MIS Department may specify the IP ADDRESS CLASS and subnet range. The Subnet Mask will be 255.255.255.0 or 255.255.0.0 depending on your network topology. A class A network would be 255.0.0.0, a class B network would be 255.255.0.0, and a Class C would be 255.255.255.0. Be aware that incorrect or inconsistent subnet mask values will cause communication problems and failures!

A subnet mask divides a network into sub networks. For example, we use 255.255.0.0, which is a Class B network. 255.0.0.0 would be Class A, and 255.255.255.0 is Class C. The 255.255.0.0 means that anyone with 10.1.xxx.xxx can communicate with each other. That is over 64,000 devices. A Class C subdivides this into 254 different networks containing up to 254 each. In any given subnet, a person can only talk to 253 other devices. Computer 10.1.207.213 cannot see a drive at 10.1.206.1 on the Class C network, but could on a Class B. This will normally be 255.255.0.0 unless the customer specifies otherwise. A subnet could be further divided; for example, 255.255.255.128, 10.1.206.1-10.1.206.127 would be one subnet and 10.1.206.129-10.1.206.254 another, not accessible by the other.

**GATEWAY ADDRESS**

X***: GWY ADDR HI:	Highest octet of the GATEWAY IP ADDRESS – range 0-255, default = 10
X***: GWY ADDR HM:	High Middle octet of GATEWAY IP ADDRESS – range 0-255, default = 1
X***: GWY ADDR LM:	Low Middle octet of GATEWAY IP ADDRESS – range 0-255, default = 205
X***: GWY ADDR LO:	Lowest octet of the GATEWAY IP ADDRESS – range 0-255, default = 3

The GATEWAY IP ADDRESS is defaulted to a value that will allow operation on the Avtron Cleveland Network. The Gateway IP Address must be set to a valid address on your network. Avtron normally sets the Gateway IP Address for all drives on a system to the Ethernet Switch's IP Address as users would be less likely to try and use the Switch IP Address by mistake. Failure to set the GATEWAY IP ADDRESS that is consistent with the DRIVE IP ADDRESS and DRIVE SUBNET MASK will result in a total loss of communications. Also,

failure to set the GATEWAY IP ADDRESS to a valid address may result in failures in communications to devices not on the drive's Subnet. Your MIS Department may want to specify the GATEWAY IP ADDRESS.

"Gateway" is a generic term for an internetworking system (a system that joins two networks together). Gateways can be implemented completely in software, completely in hardware, or as a combination of the two. We are not using gateways. The gateway address should be set to some legal IP address in the network or even the same as the drive's IP. The reason for this is that an illegal address could cause software lockup.

### **MACHINE NUMBER**

X\*\*\*: MACHINE NO: Range 0-7, default 1.

The MACHINE NO parameter is used for customer installations that have multiple ADDvantage-32 based machines (process control systems) connected to and accessible to the same ETHERNET NETWORK. The MACHINE NO parameter is only relevant to ADDAPT 2000 (ADDvantage-32 Application Programming Tools) where a Channel # from 201 to 208 must be entered in the ADDAPT configuration (ADDAPT.cfg) for each drive section. The MACHINE NO is also used in the setup of ADDAPT Real Time Screens. The ADDAPT Channel # is equal to the X\*\*\*: MACHINE NO + 200. Typically, all ADDvantage-32 drives on a specific machine/drive system would be set to the same Machine Number. ADDAPT 2000 uses both the drive's Machine Number and DRIVE ID for identifying and establishing Ethernet communication to drives for each machine/drive system within your facility.

### **WEB PASSWORD**

X\*\*\*: WEB passWrd: <<<<< FUTURE USE TO ENABLE ACCESS TO DRIVE'S WEB PAGE>>>>>

### **Drive Configure Menu – "Y" Parameters**

Y\*\*\*: ETHRNET COM: DISABLE, ENABLE, AUTO-ENABLE, default = AUTO-ENABLE

This parameter determines if the drive will communicate via ETHERNET. If this parameter is set to DISABLE or AUTO-ENABLE, then an ESBX Ethernet board is not required on the drive for correct operation. If the parameter is set to ENABLE, then an ESBX Ethernet board must be installed for the drive to operate. If there is no ESBX Ethernet board installed but the ETHRNET COM parameter is set to ENABLE, the drive may operate erratically and/or reset unexpectedly.

If ETHRNET COM is set to AUTO-ENABLE, then the drive will attempt to determine if the ESBX Ethernet board is installed as part of the power-up sequence. If the ESBX Ethernet board

is detected and correctly initialized, its presence will be indicated under the DIAGNOSTICS menu of the drive keyboard/display. The drive LCD display will show:

DRIVE COM ID:

xx (ETH)

where xx = Drive ID # and ETH indicates presence of ESBX Ethernet board.

Y083: ETH AUT-RST: DISABLE, ENABLE, default = DISABLE

MUST BE SET TO DISABLE

#### 8.4 ESBX ZAP – DOWNLOADING FIRMWARE TO ESBX ETHERNET BOARDS

The ESBX Ethernet boards contain firmware in their Flash Memory. Although not normally a field requirement, this firmware can be Field upgraded via Ethernet using Avtron's ESBX\_Zap program (PN 682937) from the source computer, usually the ADDAPT 2000 PC. Normal operation of the ESBX Ethernet board will cease upon start of ESBX ZAP which will take up to 3 minutes to complete. The ESBX board will provide indication of completion of the ZAP program by an alternating flash of CR2 and CR3 LED's. Use caution as a power cycle or drive reset during the ZAP operation or before the ZAP is complete will render the ESBX board inoperable and will require factory reprogramming at Avtron.

Zapping an ESBX board on a running drive is not totally risk free. However, there should not be a problem unless the drive is configured to generate a fault on a COM LOSS, or you have other ETHERNET devices attempting to communicate to the drive during and after the ZAP. If you are attempting to download to a failed Ethernet board whose failure symptom was a total loss in communication, then the procedure below for downloading ESBX software to the board will not work as communication with board is required. Avtron's factory can program the ESBX board without communication but it is not available for field use at this time.

The IP ADDRESS that should be entered into the ESBX ZAP program is the IP ADDRESS that is set in the "DRIVE CALIBRATION" menu. The IP ADDRESS is not programmed into the ESBX board; the ESBX board obtains its IP ADDRESS from the ADDvantage-32 drive on which it is mounted. The reason the ESBX ZAP program needs the board's IP ADDRESS is because the programming data is sent to the board via ETHERNET and the IP ADDRESS is the board address.

MAC or Media Access Control address is a unique value associated with a network adapter. MAC addresses are also known as hardware addresses or physical addresses. The MAC address remains fixed and follows the network device, but the IP address changes as the network device moves from one network to another. TCP/IP protocol is a higher level and requires the IP address.



### ESBX Ethernet Board Firmware Download Instructions:

1. Record Target ADDvantage32 drive information (Drive IP and Subnet mask addresses). From the drive keypad, enter the "Drive Calibrate" menu and record the following parameters: The "X" parameter numbers shown below are for drive application software P/N 694012 V13. Please reference Appendix C of your ADDvantage-32 Drive manual that shows the parameter listing for your specific application software.

X090: IP ADDR HI	_____
X091: IP ADDR HM	_____
X092: IP ADDR LM	_____
X093: IP ADDR LO	_____
X094: MSK ADDR HI	_____
X095: MSK ADDR HM	_____
X096: MSK ADDR LM	_____
X097: MSK ADDR LO	_____

#### NOTE

Do not enter the number 256 for X093. Use the actual DRIVE ID jumper settings on J8 as viewed for DRIVE COM ID in the drive's Diagnostic menu. If X093 does not equal 256 then use the number in X093.

2. Record the ESBX board MAC Address, located on label of U1 of the ESBX board.

MAC Address:                    \_\_\_\_ - \_\_\_\_ - \_\_\_\_ - \_\_\_\_ - \_\_\_\_ - \_\_\_\_

3. Record the Source computer's network settings information (Computer's IP and Subnet mask addresses). This information can usually be found under the Internet Protocol (TCP/IP) properties found in the Local Area Connection properties of computers Network and Dial Up Connections setup.

IP Address:	_____	:	_____	:	_____	:	_____
Subnet Mask:	_____	:	_____	:	_____	:	_____

#### NOTE

The drive and the computer's network address settings must be such that they are both capable of communicating on the same network and have a physical communication path established.

4. Execute the ESBX\_Zap program (PN 682937) from the source computer. Fill in the following information:

Drive IP Address: \_\_\_\_\_  
 Drive Download Port: 16726  
 MAC Address: \_\_\_\_\_ - \_\_\_\_\_ - \_\_\_\_\_ - \_\_\_\_\_ - \_\_\_\_\_ - \_\_\_\_\_

5. Click the "BROWSE" button and select the ESBX firmware file 682767 V12.bin or the latest version.

Avtron ADD32 ETHERNET Downloader (682937.V10)

Local Name: SKOVACIK Local IP Address: 10.1.205.200 EXIT

Drive IP Address: 10.1.205.3 Drive Download Port: 16726 Cancel

Drive MAC Address: 00 50 C2 06 E0 5Fb Send

DOWNLOAD FILE C:\682767\682767 v12.bin BROWSE

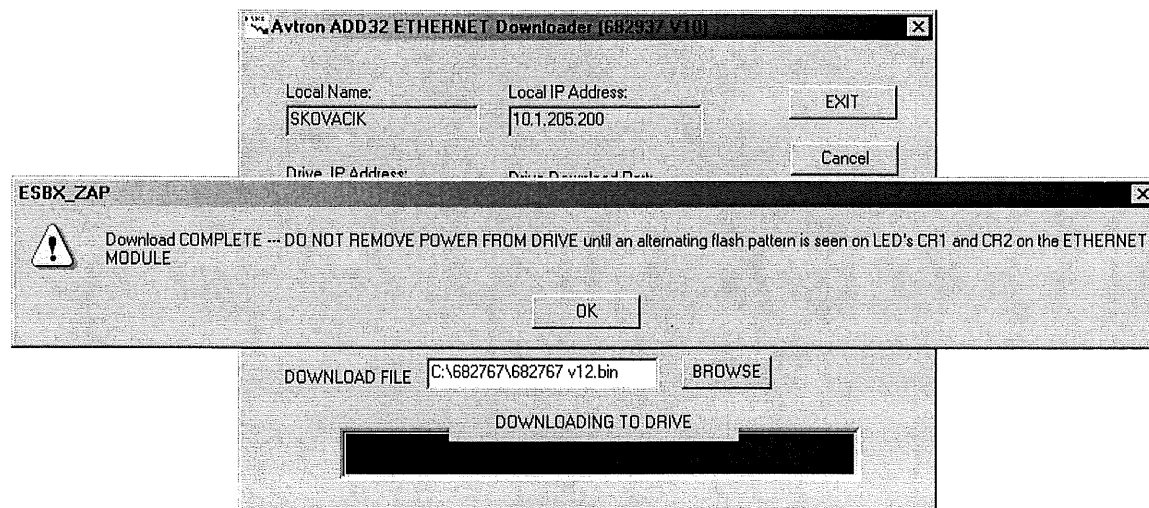
6. Click the "Send" button. A progress bar will indicate progression of file transfer. When the transfer is complete, the following dialog will appear:

\*\*\*\*\*

### WARNING

**DO NOT POWER DOWN THE DRIVE DURING AND AFTER THE DOWNLOAD UNTIL THE GREEN AND AMBER LIGHTS ON THE ESBX BOARD START TO BLINK BACK AND FORTH AT A RATE OF ABOUT ONCE PER SECOND!!!!!!**

\*\*\*\*\*



7. As indicated, once the LED's on the ESBX module are alternately flashing, indicating the firmware has been successfully transferred into non-volatile memory, perform a cold restart of the drive by removing and then re-applying control power to the drive.

## 8.5 ETHERNET SWITCHES

A Switch is a network device that connects two or more separate network segments and allows traffic to be passed between them when necessary. A Switch determines if a packet should be blocked or transmitted, based on the destination address contained in that packet. A Switch is like a hub which is an Ethernet (10BaseT or 100BaseT UTP/STP) repeater. However, a Switch does not bombard all of the ports with all data. A Switch sends incoming data only to its intended device so as to prevent collisions. Avtron provides Ethernet Switches from several different manufacturers. Please reference your Switch manual for technical information specific to your Switch model.

While most Switches do not require an IP Address assignment for operation, Avtron recommends that Switches be assigned an IP Address so that Switch diagnostic information can be obtained via Internet Explorer web pages. Avtron also normally uses the Switch's IP Address for the ADDvantage-32 drive's Gateway Address as most users would know this IP Address as being used by the Switch and would be less likely to use the address by mistake for other devices.

Some Switches are factory set with an administrative account and can be accessed over the serial link using a serial link cable provided with the Switch. The default Log In User Name and Password for many Switches is:

User Name: admin

Password: admin

Be aware that some Switches do not have an administrative account or may use a different User Name and Password than above. See your Switch manual for specific technical information. If the User Name and Password are changed from their factory default, Avtron recommends using:

User Name: avtron

Password: 64183

Once logged in via the provided serial cable, an IP address can be assigned to the Switch such that the Web-based configuration can be utilized. Many Switch manufacturers allow creation of separate user accounts with different privilege levels. In general, the default Switch configuration settings are used. The 'admin' will usually always get you in. After the initial setup of Switch IP Address via the serial cable, the Switch can be accessed by typing the IP Address as the URL in Internet Explorer.

Switch ports labeled with an X are internally crossed over. When connecting two devices, a straight through cable is used if only one device has an X. If both or neither device have an X, a Crossover cable is required. Your computer network port is not internally crossed over. Straight through CAT5 cables are used to connect your ADDAPT computer, X-link, PLC, HMI Operator Displays, Performance View, etc., to a Switch, but not to each other. Crossover cables are used to connect your computer directly to a PLC, Xlink, or even another computer or to connect two or more Switches together. Two Switches should be connected by Fiber Optic cable and simply swap connections at one end. This generally requires popping the halves of one end out of a clip, swapping, and reattaching the clip.

Ethernet Switches can be provided with a combination of both 100 MHz base Fiber Optic and 10/100 MHz UTP Copper ports with the following specifications:

100baseTX, CAT5 cable, RJ45 connector (RJ21 for mini) max length 100m

100baseFX, fiber optic, 2km full duplex (multimode cable 412m half duplex, singlemode 10km+)

For Switches that provide diagnostics using a web browser, start Internet Explorer from Windows using the ADDAPT or PLC computer on the network. Type the Switch's IP Address on the Address Line. Enter User Name and Password if required for access to the Switch Diagnostics. You may want to create a shortcut on your desktop for faster future access to the Switch's Diagnostics.

## **8.6 PLC's AND ADDAPT 2000 VIA ETHERNET COMMUNICATION**

### **8.6.1 PLC's**

The Avtron ADDvantage-32 is a high performance and highly configurable digital drive with resident capability to perform drive control functions locally utilizing a PLC for operator interface, process I/O, and permissive logic. The PLC is not burdened with time critical and

complex drive control functions yet retains the ability to communicate to the drives via a high performance Ethernet network.

Based on high speed, open Ethernet communication protocols you get the most flexibility going into the future. Avtron's ESBX Ethernet board supports the following protocols that are compatible with popular Programmable Logic Controllers (PLC's):

- Modicon: Modbus TCP
- General Electric: Ethernet Global Data, (EGD) (drive-to-drive communication with or without a PLC)  
Includes GE 90/70, 90/30 PLC's
- Designed and interfaces with Rockwell: Ethernet IP  
Type 1 (ControlLogix) Implicit Messaging  
Type 3 ControlLogix, SLC, and PLC-5 (except 5/250)  
  
Includes Allen Bradley Control Logix, PLC-5 and SLC PLC's
- Avtron Peer Primitive: Autoscan, ADDAPT, and other Avtron tool interfaces

All protocols are included with ADDvantage-32 software and all are active simultaneously. These protocols allow high-speed communication from PLC's, HMI Operator Displays, ADDAPT 2000, Avtron Performance View Process Diagnostic System, and other external devices to the ADD-32 drives as well as drive to drive. The benefits are minimized system wiring and enhanced system reliability, while retaining maximum flexibility through the life of your drive system. All Drive related system I/O (except E-Stop) can be communicated over the Ethernet network. Detailed descriptions of these protocols can be rather complex and lengthy for this user manual. Please reference the Ethernet Engineering Reports and technical Application Notes for the most recent up-to-date list of supported Ethernet protocols. This information can be obtained on Avtron's web site at <http://www.avtron.com/>.

ADDAPT 2000 and PLC programming packages can operate simultaneously on the same computer if required. It does not require two network cards inside the desktop computer to communicate to two devices, unless the two devices exist on two totally isolated networks. Note: In a Windows 2000 system, if you disable multiple network adapter (NIC) cards, then re-enable them, they are re-assigned as ports in the order they are enabled. This means you can accidentally swap the NIC's used by eth0 & eth2.

### 8.6.2 ADDAPT 2000

ADDAPT 2000 Programming Tools must be used if communicating to drives over Ethernet. ADDAPT 98 and the older ADDAPT DOS software do not support Ethernet communication. ADDAPT DOS will not work using serial link or any form of communication when drive has Ethernet Application software. Before communicating with ADDvantage-32 drives over

Ethernet using the ADDAPT 2000 Programming Tools/PC, you will need to obtain an available IP address for your ADDAPT computer. Depending on who designed the Ethernet network, you may need to get this information from the Avtron Project Engineer, your plant Project Engineer or your MIS Department. If you arbitrarily pick an IP Address, make sure that it is not used by the drives, PLC, Operator Displays, Performance View or any other device that may be connected on the network. If you are unsure if an IP Address is used, use the PING command at a DOS command prompt on a network PC.

To set your ADDAPT computer IP settings using a Win 2000 operating system, go to *Start-Settings-Control Panel-Network and Dial-up Connections*. Right click the Local Area Connection for the network board being used and select "Properties". Highlight the "Internet Protocol (TCP/IP)" and click on Properties. Check circle for "Use the following IP address". Enter the desired IP Address, Subnet Mask and Default Gateway. Click "Ok", "Ok", and Yes to reboot if prompted. Note that Windows 2000 does require rebooting the computer when changing IP settings. These IP setting instructions will be different if using a WIN 98, WIN NT or WIN XP operating system. Refer to your computer/Windows documentation if required. To see your computer's own IP Address or MAC Address, type "IPCONFIG/ALL" from a DOS command prompt.

To set up ADDAPT 2000 software for Ethernet communication, click on "Tools" – "Options". Inside the *Ethernet* tab are selections for Channels 201-208. The last digit of Channel number corresponds to the drives X102: MACHINE NO setting. Set the ADDAPT Channel # equal to the drive's Machine NO + 200. All drives in a system for a specific machine should be given the same MACHINE NO and Channel #. ADDAPT 2000 looks for all drives with the MACHINE NO and DRIVE ID corresponding to the channel(s) that are enabled. IP Address settings do not need entered into ADDAPT 2000. You must also set the Channel # for each drive section when setting the ADDAPT configuration file for the first time.

Reference your ADDAPT 2000 manual on the ADDAPT CD or in the C:\Program Files\Avtron Manufacturing\ADDAPT\Docs folder for further technical information.

## 8.7 ETHERNET COMMUNICATION TROUBLESHOOTING

In the event that you encounter any Ethernet communication problems, it will be necessary to isolate the root cause of the problem. Follow the Ethernet Troubleshooting Checklist below in the order presented. If the problem still cannot be resolved, call Avtron's Industrial Automation Field Service Department at (216) 642-1230 for further assistance. This checklist is a guide for determining where problems exist. Jot down notes for each step and present this information to the Avtron service engineer to help isolate the trouble area.

1. In what way did Ethernet board fail? Was there total loss of communication or intermittent loss of communication?

2. Are there any ADD-32 drive faults or drive LED abnormalities that may indicate a more serious drive problem? Refer to Section VII of the ADD-32 Drive Manual for LED, Power Up, and Fault definitions.
3. Has the ADD-32 ESBX board completed its 45 second boot up cycle following a power cycle?
4. Did Ethernet communication fail on one or more than one drive? If there is communication loss to multiple drives, can the problem be traced to a common Switch blade or a common Multi Fiber Cable? For communication loss to either single or multiple drives:
  - a. Measure and verify that Switch power is applied.
  - b. Is the Fiber or CAT5 Cable plugged in at both the Switch port and at the ESBX board or device end? Check connections.
  - c. Are Switch port LED's turned "on" for the section(s) with communication problems?
  - d. Temporarily move Fiber or CAT5 Cables from suspect ports to good ports. For communication loss on multiple drives, use a port on a different Switch blade. If this restores communication, the port may be bad or intermittent. Replace Switch blade or Switch.
  - e. If possible, run a temporary Fiber or CAT 5 Cable between drive(s) in question and the Switch port. If this restores communication, the cable is bad. Replace the Fiber, Multi Fiber or CAT 5 Cable.
  - f. Does cycling power to the Switch restore port communications to the drive(s)? If cycling Switch power restores communication, replace Switch blade or Switch.
5. Has the DRIVE COM ID connector been removed by mistake for connector J8 on System Maxi Board (DC Drive) or connector J6 on Microprocessor board (AC Drive)? If it has, re-install connector and **Reset** drive.
6. Has the ADD-32 drive's IP Address, Subnet Mask, or Gateway Address been changed by mistake in the "DRIVE CALIBRATE" menu? Has the drive's calibration and configuration data been defaulted by mistake? Verify all Ethernet Calibration and Configuration parameters defined in Section 8.3.2.
7. Has the Ethernet communication problem occurred following replacement of the System Maxi board? If it has, go in to the "DIAGNOSTICS" menu on the drive LCD display. Verify the ESBX PN/VER numbers. If garbage information is displayed, the Serial PROM U5 on the Maxi System board is older than the version V11 or higher required. It is also possible to observe erroneous "Bad Power Cable" drive faults. Replace Maxi board with spare containing Serial PROM U5 of V11 or higher.

8. Observe and document the LED's located on the drive's ESBX board at the time of failure:

CR1 STATUS:  
CR2 STATUS:  
RCV LED:  
TX LED:  
LINK ACTIVE LED:

9. If ESBX board LINK ACTIVE LED is "off" and Switch port LED is "off":

- a. Cycle power to ADD-32 drive and wait for the 45 second boot up to complete. Did the LINK ACTIVE LED and Switch port LED turn "on"? If so, replace the ESBX Board.

10. If ESBX LINK ACTIVE LED is "on" but communication problems still exist:

- a. Can ADDAPT 2000 and/or Performance View communicate to the drive(s)?
- b. Has another device come online in the network with a duplicate IP Address? Isolate the drive network from any other company networks.
- c. Go to a DOS command prompt and attempt to "PING" the drive(s). Use ADDAPT or PLC computer that is connected on the network. Can you ping the drive?

TYPE: ping <ip address>

EXAMPLE: ping 10.1.206.6

- d. Start Internet Explorer from Windows using the ADDAPT or PLC computer on the network. Attempt to WEB BROWSE the drive by typing the drive's IP Address on the Address Line. Did ADD-32 Web page come up?
- e. Replace ribbon cable from connector J2 on Maxi System Board to J1 connector on Microprocessor Board.
- f. Replace ESBX board on drive if it was not already replaced in step 9 above.
- g. Replace Maxi System board if DC drive.
- h. Replace Microprocessor board on DC or AC drive. Setup IP Address, Subnet Mask, and Gateway Address. If communication is now working, use ADDAPT 2000 to download drive Calibration and Configuration data.
11. For Switches that can be accessed using a web browser, start Internet Explorer from Windows using the ADDAPT or PLC computer on the network. Type the Switch's IP Address on the Address Line. Enter User Name and Password if required for access to the Switch Diagnostics. Reference your Switch manual to confirm that the ports in question are



configured to be enabled, active, and configured for the proper bandwidth. Look for diagnostics that may show port status such as errors for frame packets transmitted/received.

12. In the ADD-32 Diagnostic Menu, write down all the ETHERNET STATISTICS. Wait 5 minutes and log the ones that have changed, then wait 5 more minutes and log the ones that have changed again. You only need to write the non-zero's as blanks will be assumed to be zero. Most diagnostics should be zero. Note that the Ethernet Statistics are found under DIAGNOSTICS/VIEW ETH HISTORY on the drive LCD interface. This data may require interpretation and analysis by Avtron engineers.

DIAGNOSTIC	INIT VALUE	5 MIN	10 MIN
UDP Mpool Empty			
UDP Mpool Err			
UDP Good Receive			
UDP Invalid Type			
UDP Null			
UDP Invalid Serv			
PPR Cmd Buf Busy			
PPR Cmd Buf Rclm:			
PPR Respse Time			
PPR Reply			
PPR Overrun			
PPR Send Fail			
PPR Xmit Fail			
PPR No Reply			
QRY Frames			
QRY Responses			
QRY Overrun			
QRY Send Fail			
QRY Xmit Fail			
EXCHG Frames			
EXCHG Busy			
ASCAN Frames			
ASCAN Overrun			
ASCAN Send Fail			
ASCAN Xmit Fail			
BCAST Frames			
BCAST Busy			
BCAST Invalid			
BCAST Overrun			
BCAST Send Fail			

DIAGNOSTIC	INIT VALUE	5 MIN	10 MIN
Mb PP good rcv			
Mb PP bad rcv			
Mb PP err rcv,			
Mb PP timeout			
Mb PP good xmit			
Mb pp bad xmit			
MBus Connect Er			
MBus Max Connet			
MBus R-Connt Er			
MBus Disconnects			
MBus Invld Hdr			
MBus Rsp Snd Er			
MBus Connet 1's			
MBus Connet 2's			
MBus Connet 3's			
MBus Connet 4's			
MBus Connet 5's			
MBus Connet 6's			
MBus Connet 7's			
MBus Connet 8's			
EGD SND errors			
EGD RCV errors			
EGD CNSM Overrun			
EGD CFG Con ERR			
EGD CFG Con Good			
EGD RCV			
EGD Consume			
EGD No Match			
EXTRA 13			
EXTRA 14			
EXTRA 15			
EXTRA 16			
EXTRA 17			
EXTRA 18			
IP packets rcvd			
IP bad rcv chksm			

DIAGNOSTIC	INIT VALUE	5 MIN	10 MIN
IP too short rev			
IP too small rev			
IP hdr too short			
IP hdr bad len			
IP frag's rcv'd			
IP frags dropped			
IP frags timeout			
IP pks fwd'd			
IP can't forward			
IP fwd same net			
IP unknwn proto			
IP sent up stack			
IP local out			
IP pks dropped			
IP reasm OK			
IP frag'd OK			
IP out frg made			
IP can't frag			
IP bad options			
IP no route			
IP bad version			
IP raw ip's			
TCP Connect Init			
TCP Connect Esbl			
TCP Connect Drpd			
TCP 25			
TCP 26			
TCP 27			
TCP 28			
TCP 29			
TCP 30			
TCP 31			
TCP 32			

**ADDvantage-32 Drive Ethernet Diagnostics Definitions**

UDP Mpool Empty: software error counter. Increments if a UDP frame is received and there is no memory buffer available to hold the frame. This is an internal error. Contact Engineering if this counter is ever observed to be incrementing.

UDP Mpool Err: software error counter. Increments if the operating system returns an error in response to a request for a memory buffer. Contact engineering if this counter is ever observed to be incrementing.

UDP Good Receive: counter containing the number of valid UDP frames that have been received by the drive. In order for the UDP frame to be valid, it must have a valid footprint.

UDP Invalid Type: counter containing the number of UDP frames that were not valid. A frame will be considered invalid if it does not have a valid footprint. The probable cause of this type error will be a programming error in the device transmitting the UDP frame.

UDP Null frame: counter containing the number of UDP frames received that had a zero data length. The probable cause of this type error will be a programming error in the device transmitting the UDP frame.

UDP Invalid Serv: counter containing the number of UDP frames received that had a valid footprint but did not indicate a valid service. The probable cause of this type error will be a programming error in the device transmitting the UDP frame.

PPR Cmd Buf Busy: counter containing the number of PEER PRIMITIVE commands that were aborted due to the buffer between the ESBX and the drive being busy. This counter incrementing indicates a communication error between the ESBX module and the drive and should be reported to Engineering.

PPR Cmd Buf Rclm: counter containing the number of times that the ESBX had to reclaim the PEER PRIMITIVE buffer from the ADD-32. If this counter is incrementing, it indicates a communication error between the ESBX module and the drive and should be reported to Engineering.

PPR Respse Time: number of 5 millisecond time ticks that the ESBX module waited for a PEER PRIM response from the ADD-32. Values of 1-3 are to be expected. Values in excess of 10 should be reported to Engineering.

PPR Reply: number of valid PEER PRIM replies received from the ADD-32. This diagnostic incrementing indicates PEER PRIM communications activity to the ESBX.

PPR Overrun: counter containing the number of PEER PRIM commands that were discarded due to an overflow of the PEER PRIM command queue. Increments of this counter indicate that excessive volumes of PEER PRIM commands are being received by the ESBX module. This indicates an application problem.

PPR Send Fail: counter containing the number of failures returned by the PEER PRIM socket send operation. Increments of this counter indicate a probable network configuration problem, most likely related to the drive IP address, subnet mask, or gateway address.

PPR Xmit Fail: counter containing the number of PEER PRIM RESPONSE frame transmit failures. Increments of this counter could indicate a possible network configuration problem, (possibly related to the drive IP address, subnet mask, or gateway address) or a software related problem.

PPR No Reply: counter containing the number of times the ADD-32 did not reply to a PEER PRIMITIVE transaction initiated by the ESBX module. Increments of this counter indicate that the ADD-32 may not be responding to the ESBX and may be the result of a hardware problem or a possible software problem. Contact Engineering if this counter is incrementing.

QRY Frames: the number of QUERY frames received by the module.

QRY Responses: the number of QUERY RESPONSE frames generated by this drive. Note that a response will be generated only if a QUERY frame is received and the DRIVE ID and MACHINE number of the drive fall within the range specified by the QUERY frame.

QRY Overrun: counter containing the number of QUERY frames that were discarded due to an overflow of the QUERY command queue. Increments of this counter indicate that excessive volumes of QUERY frames are being received by the ESBX module. This indicates an application problem.

QRY Send Fail: counter containing the number of failures returned by the QUERY response socket send operation. Increments of this counter indicate a probable network configuration problem, most likely related to the drive IP address, subnet mask, or gateway address.

QRY Xmit Fail: counter containing the number of QUERY RESPONSE frame transmit failures. Increments of this counter could indicate a possible network configuration problem, (possibly related to the drive IP address, subnet mask, or gateway address) or a software related problem.

EXCHG Frames: number of EXCHANGE FRAMES received by the drive.

EXCHG Busy: counter containing the number of EXCHANGE commands that were aborted due to the buffer between the ESBX and the drive being busy. This counter incrementing indicates a communication error between the ESBX module and the drive and should be reported to Engineering.

ASCAN Frames: number of EXCHANGE FRAMES received by the drive.

ASCAN Overrun: counter containing the number of ASCAN or EXCHANGE frames that were discarded due to an overflow of the ASCAN/EXCHANGE command queue. Increments of this counter indicate that excessive volumes of ASCAN and/or EXCHANGE frames are being received by the ESBX module. This indicates an application problem.

ASCAN Send Fail: counter containing the number of failures returned by the ASCAN response socket send operation. Increments of this counter indicate a probable network configuration problem, most likely related to the drive IP address, subnet mask, or gateway address.

## 8.8 ETHERNET COMMUNICATIONS PROTOCOLS FOR ADD-32™

Ethernet communications with the ADD-32 drives are implemented using one of four common protocols or proprietary Avtron Peer-Primitives such as Avtron's ADDvantage-32 Application Programming Tools (ADDAPT™). The supported protocols are:

- Schneider Electric's Modbus TCP/IP (MB-TCP)
- GE-Fanuc's Ethernet Global Data (GE-EGD)
- Allen-Bradley's Client Server Protocol (AB-CSP), sometimes referred to as Programmable Controller Communication Commands (AB-PCCC)
- Allen-Bradley's Ethernet IP, Control/Internet Protocol (AB-CIP)

This section will describe the common concepts of Ethernet communications, network addressing and the supported protocols with the exception of the Avtron Peer-Primitives which are reserved for Avtron use such as ADDapt2000.

## 8.9 TRANSMISSION CONCEPTS

Most Ethernet communications use either the UDP or TCP formats as follows in 8.9.1 and 8.9.2.

The Requests for Comments (RFC) document series referenced below is a set of technical and organizational notes about the Internet (originally the ARPANET), beginning in 1969. Memos in the RFC series discuss many aspects of computer networking, including protocols, procedures, programs, and concepts.

### 8.9.1 User Datagram Protocol (UDP)

UDP is a standard protocol described by RFC 768, "User Datagram Protocol". UDP is an application interface to IP. It adds no reliability, flow-control, or error recovery to IP. It simply serves as a *multiplexer/demultiplexer* for sending and receiving datagrams, using ports to direct the datagrams, as shown in the following diagram.

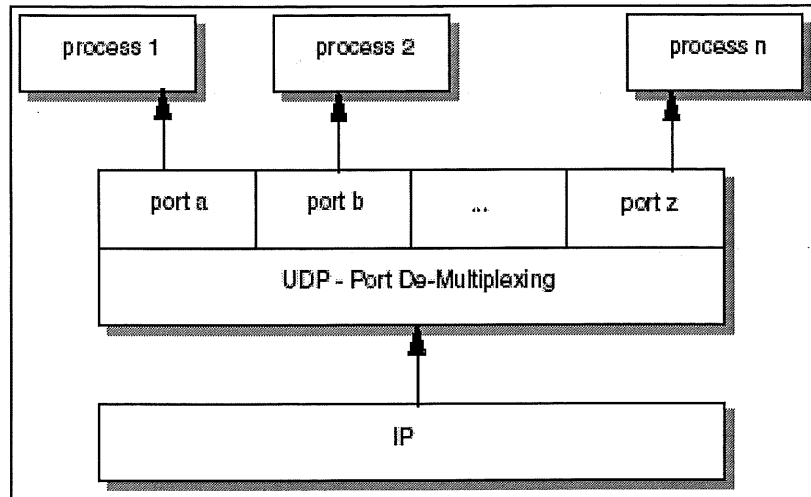


Figure 8.9.1 UDP - Demultiplexing based on ports

UDP provides a mechanism for one application to send a datagram to another. The UDP layer can be regarded as being extremely thin and consequently has low overheads, but it requires the application to take responsibility for error recovery and so on.

This format is used by the GE-Fanuc Ethernet Global Data (EGD) and Allen-Bradley Implicit Messaging.

## 8.9.2 Transmission Control Protocol (TCP)

TCP is a standard protocol described by RFC 793, "Transmission Control Protocol". TCP provides considerably more facilities for applications than UDP, notably error recovery, flow control, and reliability. TCP is a *connection-oriented* protocol, unlike UDP, which is *connectionless*. Most of the user application protocols, such as Telnet and FTP, use TCP. The two processes communicate with each other over a TCP connection (InterProcess Communication - IPC), as shown in Figure 8.9.2.

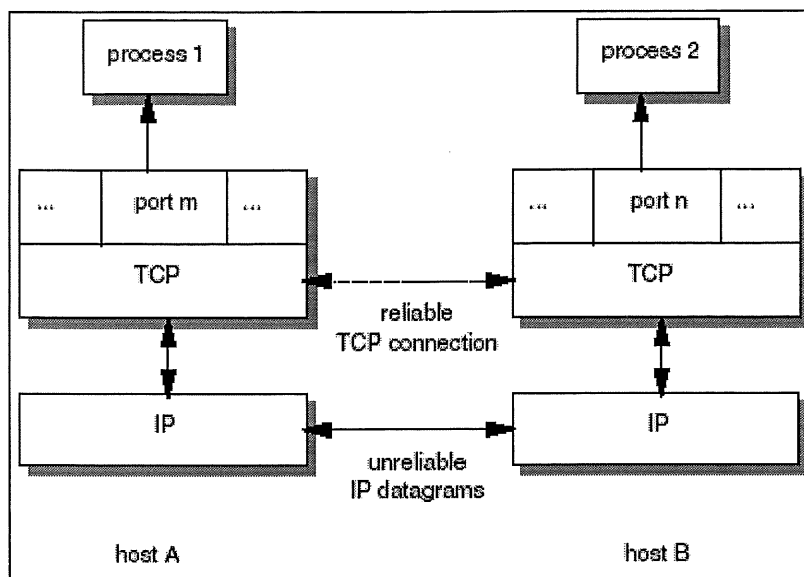


Figure 8.9.2 TCP - Connection between processes –  
(Processes 1 and 2 communicate over a TCP connection carried by IP datagrams.)

A typical set of transactions is shown in Figure 8.9.3.

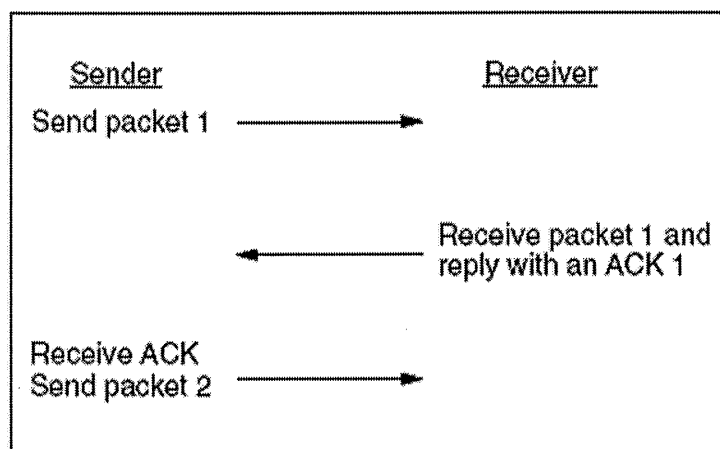


Figure 8.9.3 TCP – Transactions

This format is used by Modbus TCP and Allen-Bradley's Explicit and PCCC formats.



### 8.9.3 Network Addressing Concepts

The industry standard IP addressing definitions are as follows:

#### 8.9.3.1 Class-based IP Addresses

The first bits of the IP address specify how the rest of the address should be separated into its network and host part. The terms *network address* and *netID* are sometimes used instead of network number, but the formal term, used in RFC 1166, "Internet Numbers" is network number. Similarly, the terms *host address* and *hostID* are sometimes used instead of host number. There are five classes of IP addresses. They are shown in Figure 8.9.3.1.

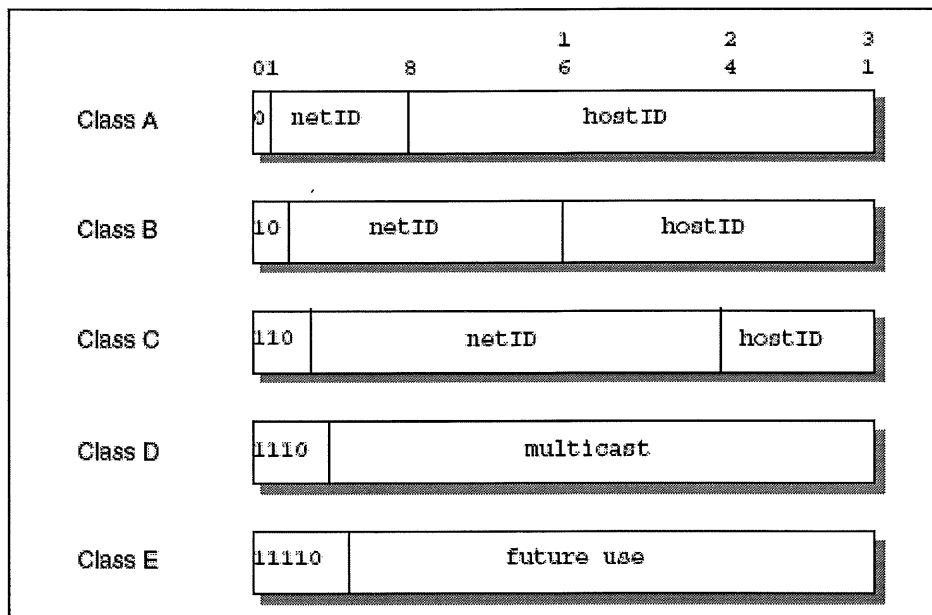


Figure 8.9.3.1 Sub-Net Classes

Where:

- Class A addresses: (1.x.x.x to 127.x.x.x), subnet mask 255.0.0.0

These addresses use 7 bits for the <network> and 24 bits for the <host> portion of the IP address. This allows for  $2^7 - 2$  (126) networks each with  $2^{24} - 2$  (16777214) hosts; a total of over 2 billion addresses.

- Loopback: The class A network 127.0.0.0 is defined as the loopback network. Addresses from that network are assigned to interfaces that process data within the local system. These loopback interfaces do not access a physical network.

- Class B addresses: (128.x.x.x to 191.x.x.x), subnet mask 255.255.0.0  
These addresses use 14 bits for the <network> and 16 bits for the <host> portion of the IP address. This allows for 2<sup>14</sup>-2 (16382) networks each with 2<sup>16</sup>-2 (65534) hosts; a total of over 1 billion addresses.
- Class C addresses: (192.x.x.x to 223.x.x.x), subnet mask 255.255.255.0  
These addresses use 21 bits for the <network> and 8 bits for the <host> portion of the IP address. That allows for 2<sup>21</sup>-2 (2097150) networks each with 2<sup>8</sup>-2 (254) hosts; a total of over half a billion addresses.
- Class D addresses: (224.x.x.x to 239.x.x.x)  
These addresses are reserved for multicasting (a type of broadcasting, but in a limited area, and only to hosts using the same class D address).
- Class E addresses: (240.x.x.x to 245.x.x.x)  
These addresses are reserved for future use.

### 8.9.3.2 Broadcast Addressing

An address with all bits one is interpreted as *all* networks or *all* hosts. For example, 128.2.255.255 means all hosts on the class B address network 128.2. This is called a directed broadcast address because it contains both a valid <network address> and a broadcast <host address>.

### 8.9.3.3 Multicast Addressing

Multicast devices use Class D IP addresses to communicate. These addresses are contained in the range encompassing 224.0.0.0 through 239.255.255.255. For each multicast address, there exists a set of zero or more hosts that listen for packets transmitted to the address. This set of devices is called a *host group*. A host that sends packets to a specific group does not need to be a member of the group. The host may not even know the current members in the group. There are two types of host groups:

- Permanent: Applications that are part of this type of group have an IP address permanently assigned by the IANA. Membership in this type of host group is not permanent; a host can join or leave the group as required. A permanent group continues to exist even if it has no members. The list of IP addresses assigned to permanent host groups is included in RFC 1700. These reserved addresses include:
  - 224.0.0.0: Reserved base address
  - 224.0.0.1: All systems on this subnet
  - 224.0.0.2: All routers on this subnet

#### 8.9.4 Interconnect Issues and Notes

- 1) All devices should be connected via a Switch; the use of hubs is not recommended. For more information on Switches vs. hubs, refer to RFC 0970, "On packet Switches with infinite storage." A non-managed Switch may be used if cost is the only issue, but the management and diagnostic capabilities of a managed Switch make the additional cost a good investment to ensure a dependable network.
- 2) The Switch port connected to an ADD-32 drive should be set to 100mb, full-duplex for best performance.
- 3) All Avtron supported protocols may be used separately or together in one system, keeping in mind not to exceed 700 frames per second. Note that TCP/IP protocols use twice the frames of UDP protocols.
- 4) The maximum data refresh rate at the drive is 8.33 mSec. In most cases, read/write repetition rates should be expressed in multiples of 10 mSec, ie: 10, 20, 50, etc.

#### 8.9.5 Avtron Supported Protocols

The following is a short overview of each of the implemented protocols. A more complete explanation of their use and programming is included in the application notes.

##### 8.9.5.1 Ethernet Communications Using EGD Protocol (GE-Fanuc's Ethernet Global Data) (GE-EGD)

The Ethernet Global Data (EGD) protocol is a protocol invented by GE-Fanuc. It may be used to connect ADD-32 drives to GE-Fanuc PLCs and other EGD compliant hardware. This protocol is an unsolicited UDP message format. Instead of a "Server" or "Client", a node on the network can be a Producer or a Consumer. The data passed between nodes on the network are passed as lists known as Exchanges. The configuration of how these lists are produced and consumed is discussed in Appendix F. The Avtron ADD-32 drives are configured using Avtron's EGDConfig program, Avtron P/N 683247. The internal data structure of the drive as data is passed from the drive's data tables is illustrated in Figure 8.9.5.1.

#### **NOTE**

Additional information on using EGD protocol is provided in Appendix F.

## ADD32-EGD INTERFACE

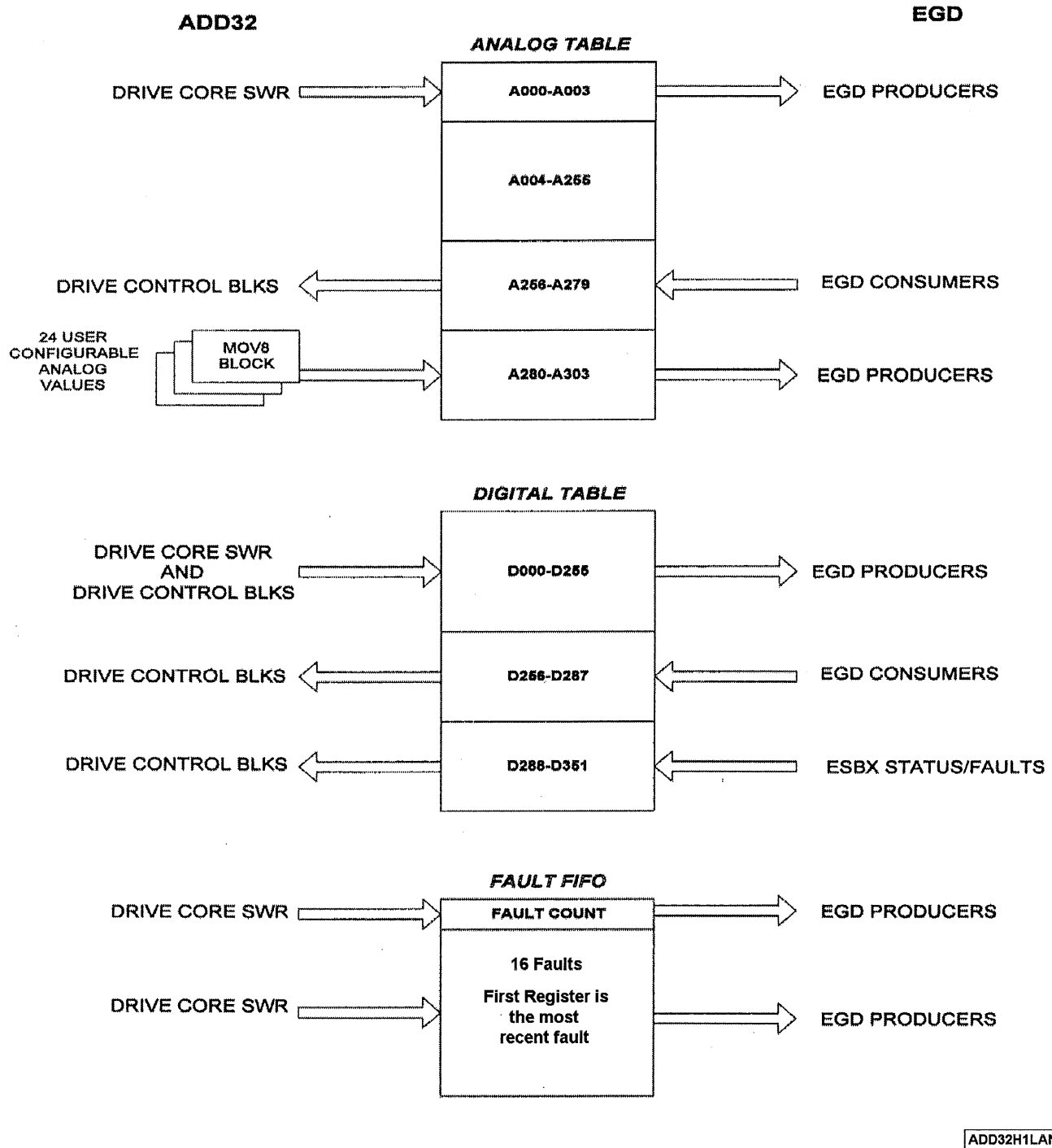


Figure 8.9.5.1 ADD-32 data transfers via EGD

EGD Exchanges are lists of data. Each node (each unique IP address) has its own list of exchanges that it can produce -- up to 32 exchanges of data. How these data lists are built and how they are interpreted at the consumer end are discussed in the Application Notes section. These Exchanges maybe configured as either Uni-Cast (Producer to a single Consumer) or Multi-Cast (Producer to a group of Consumers).

### 8.9.5.2 Schneider Electric's Modbus TCP/IP (MB-TCP)

The Modbus TCP/IP protocol was developed by Schneider Electric (Modicon) as an open standard for industrial ethernet communications. It is a Client/Server protocol of the "Master/Slave" variety, implemented via TCP/IP. This protocol can be used to connect ADD-32 drives to Modicon PLCs and other Modbus TCP/IP compliant hardware.

The Avtron implementation of Modbus TCP/IP (MB-TCP) supports the following Modbus Function Codes (MFC's):

- 1) Command Function Code= 03, Read Multiple Registers from ADD-32. This command is used to read a group of 1 to 63 consecutive registers (16 bit words) from a given address.
- 2) Command Function Code= 16, Write Multiple Registers to ADD-32. This command is used to write a group of 1 to 63 consecutive registers (16 bit words) to a given address.
- 3) Command Function Code= 01, Read Multiple Coils from ADD-32. This command is used to read a group of consecutive coils (bits) from a given address.
- 4) Command Function Code= 05, Write Coil to ADD-32. This command is used to write a single coil (1bit) to a given address.

#### NOTE

Additional information on Modbus TCP/IP is provided in Appendix G.

### 8.9.5.3 Allen-Bradley's Client Server Protocol (AB-CSP)

Allen-Bradley CSP Ethernet communications encapsulates the PCCC message structure (DF-1 style) into a packet, and delivers this packet to the PLC (or ADD-32). The CSP protocol is used predominately to talk to ADD-32 drives from PLC5 and SLC500 PLCs, programming typically done in RsLogix5 or RSLogix500. It may also be used from a ControlLogix PLC using RSLogix5000, but this is not recommended; the use of EtherNet/IP is suggested.

- For the PLC-5, the PCCC protocol supports PLC-5 Typed Writes, PLC-5 Typed Reads, and PLC-2 Unprotected Writes.
- For the SLC, the PCCC protocol supports SLC Protected Typed Logical Writes with three address fields available in the read and receive functions.

- For the ControlLogix, the PCCC protocol supports PLC-5 Typed Writes and PLC-5 Typed Reads.

#### **NOTE**

Additional information on using AB-CSP protocol is provided in Appendix H.

#### **8.9.5.4 Ethernet Communications Using Allen-Bradley Ethernet IP, Control/Internet Protocol (AB-CIP)**

Ethernet Industrial Protocol (Ethernet/IP) is an open industrial networking standard that supports implicit messaging (real-time I/O messaging) and explicit messaging (message exchange). Ethernet/IP is a further development of Allen Bradley's Common Industrial Protocol (CIP). The EtherNet/IP protocol is used to talk to ADD-32 drives from ControlNet or DeviceNet based PLCs, programming done with RSLogix5000.

Ethernet/IP consists of:

- IEEE 802.3 Physical and Data Link standard.
- Ethernet TCP/IP protocol suite (Transmission Control Protocol/Internet Protocol), the Ethernet industry standard.
- CIP, the protocol that provides real-time I/O messaging and information / peer-to-peer messaging. ControlNet and DeviceNet networks also use CIP.

TCP/IP is the transport and network layer protocol used by Explicit Messaging.

The UDP/IP (User Datagram Protocol) is used by Implicit Messaging.

#### **NOTE**

Additional information on using AB-CIP protocol is provided in Appendix I.

## SECTION IX

# SYSTEM DATA STRUCTURES

This section details the data structures of all necessary tables and data inputs used to set up and define operation of an ADDvantage-32. Some parameters are write protected, meaning the information is read only and cannot be written to. If a write is attempted on a protected area, an error message appears. All parameters, regardless of write-protect status, can be read over the serial link or 802.4 LAN.

For additional information on communicating to an ADDvantage-32, refer to Avtron Engineering Report 14363-001 for the RS-485 serial link or the Avtron ADDvantage-32 LAN Specification. These reports can be obtained upon request.

### 9.1 DATA TABLES

Information in the ADDvantage-32 is accessed using tables (Files). Each table contains a specific group of parameters or information associated with those parameters. For example, one table contains the numerical data for all the C\*\*\* parameters while a second table contains the units for these parameters.

### 9.2 DATA TABLE STRUCTURES

Data tables for the ADDvantage-32 start at number 9. Each element referenced in the table can be found by referencing its parameter number in Appendix C.

\*\*\*\*\*

#### CAUTION

Data contained in the ADDvantage-32 data tables depends on the software part number and version being used by the unit. Each software part number uses different parameters and numbers. To locate a particular parameter within a table, find the table number that contains the parameter information required. Refer to Appendix C to locate the parameter number and its position in the table.

\*\*\*\*\*

\*\*\*\*\*

## W A R N I N G

Particular locations have been set up for writing information to an ADDvantage-32. These locations are A\*\*\*:LOCATION X for analog values and D\*\*\*:LOC BIT X for digital values. It is highly recommended that all information written to an ADDvantage-32 be written to these locations. These parameters reside in regular system memory and can be written to often. If information is written to parameters such as C\*\*\*, it is being written into the EEPROM memory which has a limited number of write cycles. Although writing to the EEPROM can occur thousands of times, it is not recommended.

\*\*\*\*\*

Table 9-1 contains the data files (tables) available in the ADDvantage-32. The items listed in Table 9-1 are defined as follows:

1. File Number - Number of the table containing the data.
2. Table Name - Name of the table containing the data.
3. Structure - Number of bytes required for one element of data in the table.
4. Data Type - Data format such as:
  - FP = Floating Point Numbers (Four bytes per data element)
  - I = Integer (Two bytes per data element)
  - LI = Long Integer (Four bytes per data element)
  - A = ASCII (One byte per data element)
5. Data Mode - Data in the table is either RO or R/W.
  - RO = Read Only (Write Protected)
  - R/W = Read or Write (No Protection)
6. PAR - Represents the parameter group covered by the table.



TABLE 9-1. DATA FILES

File Number	Table Name	Structure Bytes/Element	Data Type	Data Mode	(PAR)
9	ANALOG IO	4	FP	R/W	(A000-A***)
10	ADT LABELS	11	A	RO	(A000-A***)
11	ADT UNITS	6	A	R/W	(A000-A***)
12	DEFAULT ADT UNITS	6	A	RO	(A000-A***)
13	CAL TABLE UNITS	6	A	RO	(T000-T127)
14	CAL TABLE DEFAULT	4	FP	RO	(T000-T127)
15	CAL TABLE LOW LIMITS	4	FP	RO	N/A
16	CAL TABLE HIGH LIMITS	4	FP	RO	N/A
17	CAL TABLE	4	FP	R/W	(T000-T127)
18	CONTROL CAL LABELS	11	A	RO	(C000-C***)
19	CONTROL CAL HIGH LIMITS	4	FP	RO	(C000-C***)
20	CONTROL CAL LOW LIMITS	4	FP	RO	(C000-C***)
21	CONTROL CAL DEFAULTS	4	FP	RO	(C000-C***)
22	CONTROL CONFIG LEGALS	2	I	RO	(P000-P***)
23	CONTROL CONFIG LABELS	11	A	RO	(P000-P***)
24	CONTROL CAL UNITS	6	A	R/W	(C000-C***)
25	CONTROL CONFIG	2	I	R/W	N/A
26	DEFAULT CONTROL CAL UNIT	6	A	RO	(C000-C***)
27	CONTROL CAL	4	FP	R/W	(C000-C***)
28	DIGITAL I/O	2	I	R/W	(D000-D***)
29	DDT LABELS	11	A	RO	(D000-D***)
30	DRIVE CAL LABELS	11	A	RO	(X000-X***)
31	DRIVE CAL UNITS	6	A	RO	(X000-X***)
32	DRIVE CAL HIGH LIMITS	4	FP	RO	(X000-X***)
33	DRIVE CAL LOW LIMITS	4	FP	RO	(X000-X***)
34	DRIVE CAL DEFAULTS	4	FP	RO	(X000-X***)
35	DRIVE CONFIG LABEL	11	A	RO	(Y000-Y***)
36	DRIVE CONFIG LEGALS	2	I	RO	(Y000-Y***)
37	DRIVE CONFIG	2	I	RO	(Y000-Y***)
38	DRIVE CAL	4	FP	R/W	(X000-X***)
39	SELECT LIST	11	A	RO	N/A
40	CHECK SUM	4	LI	RO	N/A
41	CAL VERSION	2	I	RO	N/A
42	DRIVE SOFTWARE AND VERSION NUMBER	2	I	RO	N/A
43	TIME ARRAY	4	LI	R/W	N/A
44	ANALYZER CAL LABELS	11	A	RO	(Z002-Z006) (Z102-Z106) (Z202-Z206) (Z302-Z306)
45	ANALYZER CAL HIGH LIM	4	FP	RO	N/A
46	ANALYZER CAL LOW LIMITS	4	FP	RO	N/A
47	ANALYZER CAL DEFAULTS	4	FP	RO	N/A
48	ANALYZER CAL	4	FP	R/W	N/A

TABLE 9-1. DATA FILES (Cont.)

File Number	Table Name	Structure Bytes/Element	Data Type	Data Mode	(PAR)
49	ANALYZER CONFIG PROMPT	11	A	RO	(Z002-Z006) (Z102-Z106) (Z202-Z206) (Z302-Z306)
50	ANALYZER CONFIG LEGALS	2	I	RO	N/A
51	ANALYZER CONFIG	2	I	R/W	(Z007-Z0**) (Z107-Z1**) (Z207-Z2**) (Z307-Z3**)
52	DIAGNOSTIC STATUS CHAN-1	2	I	RO	N/A
53	DIAGNOSTIC STATUS CHAN-2	2	I	RO	N/A
54	DIAGNOSTIC STATUS CHAN-3	2	I	RO	N/A
55	DIAGNOSTIC STATUS CHAN-4	2	I	RO	N/A
56	DIAG. TRACE DATA CHAN-1	4	FP	RO	N/A
57	DIAG. TRACE DATA CHAN-2	4	FP	RO	N/A
58	DIAG. TRACE DATA CHAN-3	4	FP	RO	N/A
59	DIAG. TRACE DATA CHAN-4	4	FP	RO	N/A
60	RETURN FAULTS	2	I	RO	N/A
61	KEYBOARD/DISPLAY MODE	2	I	R/W	N/A
62	VIRTUAL KEYBOARD DISPLAY	1	A	R/W	N/A
63	DOWNLOADING	2	I	R/W	N/A
64	RETURN FAULTS	2	I	R/W	N/A
65	ARM TRACE	2	I	R/W	N/A
66	TRACE	2	I	RO	N/A
67	FTRACE	2	I	RO	N/A
68	LINK CONTROL BITS	2	I	R/W	N/A

### 9.3 FILE NUMBER DESCRIPTION

The files listed in Table 9-1 are described as follows.

#### 9.3.1 FILE 9 - ANALOG I/O

This file defines the analog data table where computed analog data values are stored in floating point format. This table contains application specific data where size and definition are functions of the software part number and the drive application.

#### 9.3.2 FILE 10 - ADT LABELS

Contains all of the predefined label definitions for each analog input listed in File 9.

Typical values could be:

First element - FIL\_SPEED\_\_ (spaces are shown as \_\_)

Next element - FIL\_ARM\_CUR

Reading the first element of File 10 would return the following data

..... 46H 49H 4CH 20H 53H 50H 45H 45H 44H 20H 20H ....

F I L S P E E D

### 9.3.3 **FILE 11 - ADT UNITS**

Contains the units associated with each of the labels defined in File 10.

Typical values could be:

First element - \_\_FPM\_

Reading this element would return the following data

..... 20H 20H 46H 50H 4DH 20H .....

F P M

This file may be written to and used to modify the units display. Sending a write message for this table and the first element of

..... 20H 20H 59H 50H 4DH 20H .....

Y P M

would modify the display units to be YPM instead of FPM.

### 9.3.4 **FILE 12 - DEFAULT ADT UNITS**

This file contains the default units for the corresponding analog input elements.

### 9.3.5 **FILE 13 - CAL TABLE UNITS**

This file contains all of the calibration unit definitions for the corresponding calibration element of the X-Y taper tables. This table organization differs from the normal organization. The corresponding calibration tables, File 14 and File 17, contain 128 elements total, but they are organized as four sub-tables of 32 elements each. (Refer to Files 14 and 17.)

### 9.3.6 **FILE 14 - CAL TABLE DEFAULTS**

This file contains all of the predefined default values for calibration.

The organization of this file differs in that the complete table is broken up into four sub-files. Each sub-file is organized as one floating point value grouped in sub-files of 32 elements each. For example:

Sub-File 0

Value

element 0	FP
1	FP
.	.
element 31	FP

Sub-File 1	Value
element 32	FP
.	.
.	.
element 63	FP

### 9.3.7 **FILE 15 - CAL TABLE LOLIM**

This file contains the one predefined low limit value for all calibration entries. The element contains the value of -9999.0 as the low limit value. Any calibration entry must be greater than this value.

### 9.3.8 **FILE 16 - CAL TABLE HILIM**

This file contains the one predefined high limit value for all calibration entries. The element contains the value of +9999.0 as the high limit value. Any calibration entry cannot exceed this maximum value.

### 9.3.9 **FILE 17 - CAL TABLE**

This file contains all of the calibration values for each entry in the calibration file. Before writing any value to this file, check the value against the low and high limit values to insure that it is within limits. The write procedures in the receiving station do not check to see if a value is within limits. The organization of this file also differs in that the complete file is broken up into four sub-files. Each sub-file is organized as one floating point value grouped in 32 elements. For the file organization, refer to File 14.

On default initialization, the default values are copied from File 14 into this File. The user may modify the values which will then be used at all future power up conditions, unless the default power up is repeated.

### 9.3.10 **FILE 18 - CONTROL CAL LABELS**

This file contains all predefined label definitions for the control calibration. One element is used to produce one label. For example:

First element - ZERO\_ANALOG (spaces are shown as \_\_)  
 Next element - ONE\_ANALOG\_

Reading the first element returns the following data:

..... 5AH 45H 52H 4FH 20H 41H 4EH 42H 4CH 4FH 47H ....  
 Z E R O A N A L O G

### 9.3.11 **FILE 19 - CONTROL CAL HI LIMS**

This file contains all of the predefined high limit values for each control calibration value.

9.3.12 **FILE 20 - CONTROL CAL LO LIMS**

This file contains all of the predefined low limit values for each control calibration value.

9.3.13 **FILE 21 - CONTROL CAL DEFAULTS**

This file contains all of the predefined default values for control calibration.

9.3.14 **FILE 22 - CONTROL CONFIG LEGALS**

This file contains the drive configuration legal and is organized as a two-dimensional array of eight integer values per element with 139 elements maximum. Each element of eight values represents the legal choices that may be selected for that particular element of configuration in File 25.

9.3.15 **FILE 23 - CONTROL CFG LABELS**

This file contains the drive configuration labels. One element is used to produce one label.

For example:

First element - JOG REF

Next element - MASTER REF

9.3.16 **FILE 24 - CONTROL CAL UNITS**

This file contains the units associated with each of the labels defined for the control calibration values. One element is used to define one unit.

9.3.17 **FILE 25 - CONTROL CONFIG**

This file contains the control configuration data for the particular drive software version and part number.

9.3.18 **FILE 26 - DEFAULT CONTROL CAL UNITS**

This file contains all of the predefined default units for control calibration. One element is used to define one unit definition.

For example:

First element - UNITS

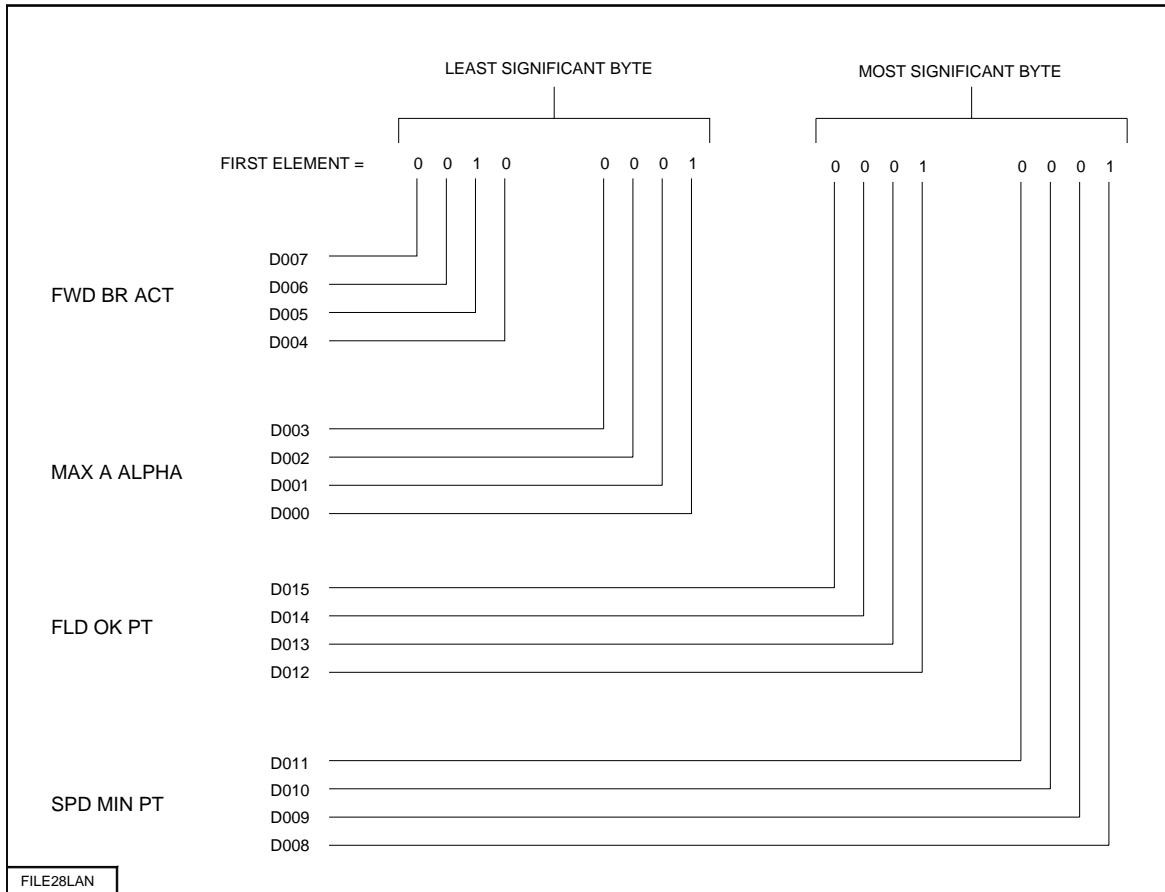
Next element - UNITS

9.3.19 **FILE 27 - CONTROL CAL**

This file contains all of the calibration values for each control calibration entry. Each element contains one calibration value in floating point format. This file will be loaded with the contents of File 21 at initial power up, and if the drive is defaulted.

9.3.20 **FILE 28 - DIG IO**

This file defines the digital data table. Each bit in the structure represents real time digital data. A bit set equal to one (1) indicates an “ON” condition, while a zero (0) indicates an “OFF” condition.



The illustrated example for File 28 shows that the Forward Bridge is active and maximum firing angle has been reached. Additionally, the motor field feedback is within the 10% setpoint and the drive is configured for the contactor to remain sealed (upon RUN removal) until ZERO SPEED.

### 9.3.21

#### **FILE 29 - DDT LABELS**

This file contains all predefined label definitions for the digital data table.

One element is used to produce one label. For example:

First element - MAX\_A\_ALPHA (spaces are shown as \_\_)

Next element - MIN\_A\_ALPHA

### 9.3.22

#### **FILE 30 - DRIVE CAL LABELS**

This file contains all predefined label definitions for the drive calibration. One element is used to produce one label.

For example:

First element - I/O\_V-REF

Next element - MOTOR\_IARM

### 9.3.23 **FILE 31 -DRIVE CAL UNITS**

This file contains the units associated with each of the labels defined in Table 30 for drive calibration. One element is used to define the units for the associated label.

For example:

First element - VOLTS

Next element - %\_DRIVE

### 9.3.24 **FILE 32 - DRIVE CAL HI LIMS**

This file contains all of the predefined high limit values for each drive calibration value. Each element contains one high limit value.

### 9.3.25 **FILE 33 - DRIVE CAL LO LIMS**

This file contains all of the predefined low limit values for each drive calibration value. Each element contains one low limit value.

### 9.3.26 **FILE 34 - DRIVE CAL DEFAULTS**

This file contains all of the predefined default values for drive calibration. Each element contains one default drive calibration value.

For example:

First element - -7.00

Next element - 10.0

### 9.3.27 **FILE 35 - DRIVE CONFIG LABEL**

This file contains the drive configuration labels displayed during drive configuration. Each element contains one label.

For example:

First element - DRIVE\_PN

Next element - BRIDGE\_SELFTEST

### 9.3.28 **FILE 36 - DRIVE CONFIG LEGALS**

This file contains the drive configuration legal options.

The two bytes per element are grouped as shown:

bit	15 14 13 12	11 10 09 08 07 06 05 04 03 02 01 00
	Type	Index Value

The upper four bits define the type assigned, while the lower 12 bits define the index into the file elements defined by the type. For example, if the type bits were 03, then the index value would be the offset into the drive calibration table. Examples of type bits are as follows:

<u>TYPE</u>	<u>File</u>
0	Select List
1	Analog Data Table
2	Digital Data Table
3	Drive Calibration
4	Control Calibration
5	Drive Configuration
6	Control Configuration

#### 9.3.29 **FILE 37 - DRIVE CONFIG**

This file contains the drive configuration settings. The file is organized the same as File 36.

For example:

First element - DRIVE\_PN  
Next element - BRIDGE\_SELFTEST

#### 9.3.30 **FILE 38 - DRIVE CAL**

This file contains all of the calibration values for each drive calibration entry. At initial power up, or a power up with default conditions request, the default values in File 34 will be written into this file.

For example:

First element - AD\_REF  
Next element - IARM\_SPAN

#### 9.3.31 **FILE 39 - SELECT LIST LABELS**

The select list table contains ASCII data that may be read, but not written to.



Each element in this table contains generic alpha labels that may be displayed for a number of different variables. Some examples are as follows:

First element   DISABLED    
 Next element   ENABLED  

### 9.3.32 **FILE 40 - CHECKSUM AREA**

This file contains the checksum values for each of the six calibration and configuration areas.

Each element is an unsigned long integer value. (Refer to section 6.2 of ER 14363-001 for recovery of long integers.) The checksum and element assignment are as follows:

<u>CHECKSUM AREA</u>	<u>ELEMENT NUMBER</u>
Drive Calibration	0
Control Calibration	1
Drive Configuration	2
Control Configuration	3
Calibration	4
Analyzer Calibration	5
Analyzer Configuration	6

### 9.3.33 **FILE 41 - CAL VERSION**

This file consists of one integer element containing the version number of the calibration data.

### 9.3.34 **FILE 42 - SOFTWARE PART NUMBER AND VERSION NUMBER**

This file contains the part number and version number for the particular version installed in the unit.

The table is organized as two bytes per element with two integer elements. They are organized as:

Part Number	Element 0
Version	Element 1

Reading this file would return the part number and version number of the installed software.

### 9.3.35 **FILE 43 - TIME ARRAY**

This file is organized as two long integer values of four bytes each. The lower element value is a time reference that may be written with a time reference value by the master station. If it is not written to, it will default to a value of zero (0). The upper element value will be incremented six times for each line cycle after the time reference is set. Each element is an unsigned long integer value. (Refer to section 6.2 of ER 14363-001 for recovery and writing to elements containing long integers.)

Integer 0 - Time reference value  
 Integer 1 - Time intervals since last time reference.

### 9.3.36 **FILE 44 - ANALYZER CAL LABELS**

This file contains the analyzer calibration labels. Each of the four groups (Channels 1 through 4) is made up of eight elements.

For example:

First element - TRIG LEVEL 1  
 Next element - RATE 1

### **NOTE**

While scrolling through the ADDvantage-32™ keypad in the ANALYZER SETUP menu, parameters Z000:RESET 1 and Z001:OUTPUT 1 appear. Z000, Z001, Z100, Z101, Z200, etc., are not included elements in this file. The RESET and OUTPUT functions are only available when executed on the keypad.

### 9.3.37 **FILE 45 - ANALYZER CAL HI LIMS**

This file contains the analyzer calibration high limit values. This file contains eight floating point values for each of the four channels in File 44. Data limits for each channel are identical. Elements 0-4 correspond to (Z002-Z006). Elements 8-12 correspond to (Z102-Z106), etc.

### EXAMPLE: **ANALYZER CAL HI LIMS - FILE 45**

Analyzer 1		Analyzer 2	
Element		Element	
0	9999.0	8	9999.0
1	9999.0	9	9999.0
2	2999.0	10	2999.0
3	9999.0	11	9999.0
4	9999.0	12	9999.0
5	0.0	13	0.0
6	0.0	14	0.0
7	0.0	15	0.0

Analyzer 3		Analyzer 4	
Element		Element	

16	9999.0	24	9999.0
17	9999.0	25	9999.0
18	2999.0	26	2999.0
19	9999.0	27	9999.0
20	9999.0	28	9999.0
21	0.0	29	0.0
22	0.0	30	0.0
23	0.0	31	0.0

### 9.3.38 **FILE 46 - ANALYZER CAL LO LIMS**

This file contains the analyzer calibration low limit values for each of the four channels in File 44. Data limits for each channel are identical. See Section V.

### 9.3.39 **FILE 47 - ANALYZER CAL DEFAULTS**

This file contains the analyzer calibration default values for each of the four channels in File 44 that will be loaded into calibration on initial power up. Data values for each channel are identical. See Section V.

### 9.3.40 **FILE 48 - ANALYZER CAL**

This file contains the actual calibration values used for each of the four channels in File 44 to process the collected analyzer data. The default values initially used for each channel are identical. On default initialization, the default values from File 47 are copied into this file. The user may modify the values which will then be used at all future power up conditions unless the default initialization is repeated. See Section V.

### 9.3.41 **FILE 49 - ANALYZER CONFIG LABEL**

This file contains the analyzer configuration prompts. (Refer to File 51.)

### 9.3.42 **FILE 50 - ANALYZER CONFIG LEGALS**

This file contains analyzer configuration legal data.

This file contains the legal references that may be used to configure control for each channel. This table must be used to generate configuration data changes. Any data reference not contained in this table will be invalid, and control action will be undefined. The table is organized as a two-dimension array with eight (8) by nineteen (19) unsigned short integer values for each of the four channels. Each of the tables consists of a maximum of eight choices for each of the nineteen variables.

### **NOTE**

See Appendix A of Serial Link Specification, ER 14363-001 - Table 50 for valid values, and note that some are unused.

Channel 1:

choice 0      choice 1 .....choice 8

VARIABLE

Element 0	(SELECT_TYPE + RISING),.....,EOLST
Element 1	. . .
.	. . .
.	. . .
.	. . .
.	. . .
Element 18	(SELECT_TYPE + FALLING),.....,EOLST

9.3.43

**FILE 51 - ANALYZER CONFIG**

This file contains analyzer configuration data. Writing to this table changes the configuration of the channel being monitored and the control variables for each of the four channels. The valid control configuration data is contained in File 50. This file is organized as 19 unsigned short integer values for each of the four channels, for a total of 76 elements.

Channel 1:

VARIABLE

First element - ENABLE\_REC1

Next element - INP1\_A/D

.
.
.

Last element

Channels 2 through 4 are identical in form.

9.3.44

**FILES 52 THROUGH 55 - DIAGNOSTIC STATUS TABLES**

The diagnostic status tables allow recovery of the status of each of the four diagnostic channels, Files 56 through File 59. Refer to section 8.19 of ER 14363-001. The complete status data must be recovered to determine the status and state of the diagnostic data table before reading any data table. The data from the data tables may not be read until the status indicates that the data sampling and storage is complete and ready for recovery. The file number assignments are as follows:

File 52	-	The status of channel 1 - Data file 56
File 53	-	The status of channel 2 - Data file 57
File 54	-	The status of channel 3 - Data file 58
File 55	-	The status of channel 4 - Data file 59

Each of the four status files are organized as a collection of integers and floating point data elements.

52	DIAGNOSTIC STATUS- CHAN 1	2	I	RO
53	DIAGNOSTIC STATUS- CHAN 2	2	I	RO
54	DIAGNOSTIC STATUS- CHAN 3	2	I	RO
55	DIAGNOSTIC STATUS- CHAN 4	2	I	RO

## 9.3.45

**FILES 56 THROUGH 59 - DIAGNOSTIC TRACE DATA TABLES**

56	DIAGNOS. TRACE DATA- CHAN 1	4	FP	RO
57	DIAGNOS. TRACE DATA- CHAN 2	4	FP	RO
58	DIAGNOS. TRACE DATA- CHAN 3	4	FP	RO
59	DIAGNOS. TRACE DATA- CHAN 4	4	FP	RO

## 9.3.46

**FILE 60 - FAULT TABLE**

This file contains the drive fault FIFO and is organized as 16 short integer elements. Each element may contain one fault value detected by the drive.

60	RETURN FAULTS	2	I	RO
----	---------------	---	---	----

Each table element is defined as follows:

bit	15 14 13 12	11 10 09 08 07 06 05 04 03 02 01 00
	Type	Index Value

The upper four bits define the type assigned, while the lower 12 bits define the index into the table defined by the type. For example, if the type bits were 00, then the index value would be the offset into the Select List table. The defined types and tables are as follows:

<u>TYPE</u>	<u>TABLE</u>
0	Select List

1	Analog Data Table
2	Digital Data Table
3	Drive Calibration
4	Control Calibration
5	Drive Configuration
6	Control Configuration
7	Reserved
8	Unused
9	Unused
10	Unused
11	Unused
12	Unused
13	Unused
14	Unused
15	Unused

**NOTE**

For File 60, the type bits must be set at 00 to view faults. Faults only reside in the Select List table.

9.3.47

**FILE 61 THROUGH 62 KEYBOARD/DISPLAY MODE TABLES**

61	KEYBOARD/ DISPLAY MODE	2	I	R/W
----	------------------------------	---	---	-----

**NOTE**

*When writing to file 61 using the Allen-Bradley Client Server Protocol (AB-CIP), the data packet received by the ADDvantage32 will be regarded as an AutoScan Write, with the expected data structure as given within Table 9.3.47-1 below. A sample RSLogix 5<sup>TM</sup> MSG (message) block configuration for performing an AutoScan Write is given in Figure 9.3.47-1. Reference Appendix H for further information regarding the AB-CSP protocol.*

61	AUTOSCAN WRITE	Up to 24	I	W
----	----------------	----------	---	---

Expected Data Packet Format:

**Word.Bit    Description:**

0	Analog Setpoint Data Starting Address (Word 1)
1	Analog Setpoint Data Starting Address (Word 2)
2	Digital Setpoint Data Starting Address (Word 1)
3	Digital Setpoint Data Starting Address (Word 2)
4	Digital Setpoint to ADDvantage32
4.1	Digital Setpoint to ADDvantage32
4.2	Digital Setpoint to ADDvantage32
4.3	Digital Setpoint to ADDvantage32
4.4	Digital Setpoint to ADDvantage32
4.5	Digital Setpoint to ADDvantage32
4.6	Digital Setpoint to ADDvantage32
4.7	Digital Setpoint to ADDvantage32
4.8	Digital Setpoint to ADDvantage32
4.9	Digital Setpoint to ADDvantage32
4.1	Digital Setpoint to ADDvantage32
4.11	Digital Setpoint to ADDvantage32
4.12	Digital Setpoint to ADDvantage32
4.13	Digital Setpoint to ADDvantage32
4.14	Digital Setpoint to ADDvantage32
4.15	Digital Setpoint to ADDvantage32
5	RESERVED 0x00
6	Number of Analog Setpoints (Word 1)
7	Number of Analog Setpoints (Word 2)
8 & 9	Analog Setpoint to ADDvantage32
10 & 11	Analog Setpoint to ADDvantage32
12 & 13	Analog Setpoint to ADDvantage32
14 & 15	Analog Setpoint to ADDvantage32
16 & 17	Analog Setpoint to ADDvantage32
18 & 19	Analog Setpoint to ADDvantage32
20 & 21	Analog Setpoint to ADDvantage32
22 & 23	Analog Setpoint to ADDvantage32

**Table 9.3.47 - 1**

- The Analog Setpoint Data Starting Address refers directly to the analog data table address where the Analog Setpoint values will be consecutively written. The Analog Setpoint Data Starting Address is interpreted as a 32-bit integer, with Word 1 being the least significant, Word 2 as most significant. For example, placing a value of 42 in Word 1 a value of 0 in Word 2, the analog data table address will be identified as A042:. Typical applications use A####:LOCATION 1 through A####:LOCATION 8 for this purpose. The analog setpoints must be of 32-bit IEEE 485 format, little endian, and occupy two consecutive 16-bit integer registers at the locations given in Table 9.3.47-1. The number of Analog Setpoint values written is scalable using the Number of Analog Setpoints parameter. The Number of Analog Setpoints is interpreted as a 32-bit integer, with Word 1 being the least significant, Word 2 as most significant. This value can be up to 8 floating point values and will determine the overall size of the message. As an example, if only two analog values are intended to be sent as part of the AutoScan Write message, the Number of Analog Setpoints parameter shall be set to two (2) and the total message length transferred to the ADDvantage32 should therefore be 12 integer words in length.

- The Digital Setpoint Data Starting Address refers to the digital data table address where the Digital Setpoint bits will be consecutively written. The Digital Setpoint Data Starting Address is interpreted as a 32-bit integer, with Word 1 being the least significant, Word 2 as most significant. For example, placing a value of 96 in Word 1 a value of 0 in Word 2, the digital data table address will be identified as D096:. Typical applications use D###:LOC BIT 1 through D###:LOC BIT 16 for this purpose. The number of digital setpoints is fixed at 16 and occupy integer word #4 within the AutoScan Write message.

RSLogix 5™ MSG configuration for AutoScan Write:

The screenshot shows the 'MSG - Rung #2:0 - MG100:0' window with the 'General' tab selected. The configuration is as follows:

Section	Field	Value
This PLC-5	Communication Command	PLC-5 Typed Write
	Data Table Address	N7:0
	Size in Elements	24
	Port Number	2
Target Device	Data Table Address	N61:0
	MultiHop	Yes
Control Bits	Ignore if timed out (TO)	0
	To be retried (NR)	0
	Awaiting Execution (EW)	0
	Continuous Run (CO)	0
	Error (ER)	0
	Message done (DN)	1
Error	Message Transmitting (ST)	0
	Message Enabled (EN)	0
Error Description	Error Code(Hex)	0

The 'Error Description' field at the bottom shows 'No errors'.

Figure 9.3.47 - 1



**NOTE**

*Reading File 61 using the Allen-Bradley Client Server Protocol (AB-CIP), will be regarded as an AutoScan Read by the ADDvantage32, with the return data packet structured as given in Table 9.3.47-2 below. A sample RSLogix 5™ MSG (message) block configuration for performing an AutoScan Read is given in Figure 9.3.47-1. Reference Appendix H for further information regarding the AB-CSP protocol.*

61                      AUTOSCAN READ                      Up to 36                      I                      R

Response Data Packet Format:

Word.Bit	Description:
0 & 1	Analog Feedback from ADDvantage32: A000: FIL SPEED
2 & 3	Analog Feedback from ADDvantage32: A001: FIL ARM CUR
4 & 5	Analog Feedback from ADDvantage32: P###: AUTOSCAN 1
6 & 7	Analog Feedback from ADDvantage32: P###: AUTOSCAN 2
8 & 9	Analog Feedback from ADDvantage32: P###: AUTOSCAN 3
10 & 11	Analog Feedback from ADDvantage32: P###: AUTOSCAN 4
12 & 13	Analog Feedback from ADDvantage32: P###: AUTOSCAN 5
14 & 15	Analog Feedback from ADDvantage32: P###: AUTOSCAN 6
16	Digital Feedback from ADDvantage32: D000: thru D015:
17	Digital Feedback from ADDvantage32: D016: thru D031:
18	Digital Feedback from ADDvantage32: D032: thru D047:
19	Digital Feedback from ADDvantage32: D048: thru D063:
20	Digital Feedback from ADDvantage32: D064: thru D079:
21	Digital Feedback from ADDvantage32: D080: thru D095:
22	Digital Feedback from ADDvantage32: D096: thru D111:
23	Digital Feedback from ADDvantage32: D112: thru D127:
24	Digital Feedback from ADDvantage32: D128: thru D143:
25	Digital Feedback from ADDvantage32: D144: thru D159:
26	Digital Feedback from ADDvantage32: D160: thru D175:
27	Digital Feedback from ADDvantage32: D176: thru D191:
28	Digital Feedback from ADDvantage32: D192: thru D207:
29	Digital Feedback from ADDvantage32: D208: thru D223:
30	Digital Feedback from ADDvantage32: D224: thru D239:
31	Digital Feedback from ADDvantage32: D240 thru D255:
32	Digital Feedback from ADDvantage32: D256: thru D271:
33	Digital Feedback from ADDvantage32: D272: thru D287:
34	Digital Feedback from ADDvantage32: D288: thru D303:
35	Digital Feedback from ADDvantage32: D2304: thru D319:

**Table 9.3.47 - 2**

- The Analog Feedback data will be returned as 32-bit IEEE 485 format, little endian and occupy two consecutive 16-bit integer registers at the locations given in Table 9.3.47-2. The number of Analog Feedback values is fixed at 8.
- The Digital Feedback data starts at the beginning of the digital data table (D000:), in 16-bit integral blocks who's length is determined by the requested length of the AutoScan Read message. For example, if an AutoScan Read

with a length of 20 registers is requested, the ADDvantage32 will return a packet 20 integers in length, where the first 16 integers contain Analog Feedback data and the remaining four integers contain Digital Feedback data D000: through D063:

RSLogix 5™ MSG configuration for AutoScan Read:

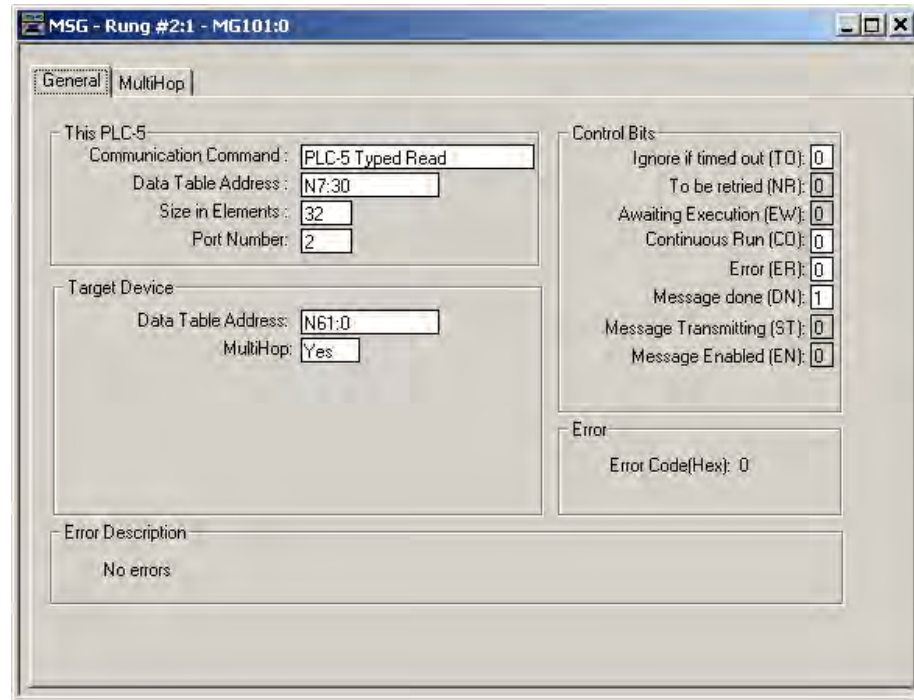


Figure 9.3.47 - 2

62	VIRTUAL KEYBOARD DISPLAY	1	A	R/W
----	-----------------------------	---	---	-----

#### 9.3.48 **FILE 63 THROUGH 64 MISC. STATUS FILES**

63	DOWNLOADING	2	I	R/W
64	RETURN FAULTS	2	I	R/W

#### 9.3.49 **FILE 65 THROUGH 68 DIAGNOSTIC TRACE CONTROL FILES**

65	ARM TRACE ENABLE	2	I	R/W
66	TRACE	2	I	RO
67	FTRACE	2	I	RO
68	LINK CONTROL	2	I	R/W

## **SECTION X**

# **SERIAL LINK INSTALLATION AND TROUBLESHOOTING**

This section contains drawings and tables useful when installing and troubleshooting a serial link.

Drawing B22068 sheets 1, 3, and 5 show ADD-32 serial link wiring.

Table 10-1 provides a list of RS232 pin assignments for connectors DB9 and DB25.

Table 10-2 provides a list of potential problems along with possible causes and remedies.

### **SERIAL DATA FORMAT**

1. One Start Bit (logic level low)
2. Eight Data Bits, least significant bit first (Bit 0)
3. One Parity Bit (even parity)
4. One Stop Bit (logic level high)

REVISIONS									
ECN NO.	LTR	DESCRIPTION	DATE	APPROVED					
26240	A	REV SHITS 1-3 PER ECN	DZIMOVIC 11/25/91	JB 11/27					

**NOTE:** ADDVANTAGE-32 SERIAL LINK ADDRESSING  
THE ADD-32'S ADDRESS IS SET AS A BINARY NUMBER USING JUMPERS ON CONNECTOR J5 (MINI-SYSTEM BOARD) OR J8 (MAXI-SYSTEM BOARD). IN BOTH CASES ID00 IS THE "LSB" AND ID7 IS THE "MSB". SERIAL LINK ADDRESS ZERO, 0, REQUIRES NO JUMPERS.

OPTO 22  
AC24 AT

AVIRON P/N - 347749  
VENDOR P/N - AC24 AT

1) JUMPER GROUP (A) COMMUNICATION PORT HARDWARE ADDRESS IS SET TO (2000) HEX

2) INTERRUPT JUMPER GROUP COMMUNICATION PORT INTERRUPT IS SET TO (IRO5) WITH (CTS) "CLEAR TO SEND" LINE DISABLED.

3) JUMPER GROUPS (B & C) COMMUNICATIONS PORT HARDWARE CONFIGURATION SETUP FOR SINGLE POINT OR MULTI-DROP SERIAL LINK WITH ADDVANTAGE-32 DRIVE(S).

ADD-32 SERIAL LINK WIRING

AVIRON MFG. INC.  
7980 E. PLEASANT VALLEY RD.  
INDEPENDENCE, OH 44131 - 5529

DATE: 9-16-91  
DRAWN: L. MARTIN  
CHECKED: [ ]  
ENG. APP'D: NITRO  
APP'D. PROD.: SLITVAK

USED ON: [ ]  
NEXT ASSEMBLY: [ ]

MODEL: [ ]

ADD-32 SERIAL LINK WIRING

SIZE: B  
DWC NO.: B22068  
SH: 1  
OF: 5  
REV: A

IMF ☒ PSF ☐

Figure 10-1. ADD-32 Serial Link Wiring (Sheet 1 of 3)

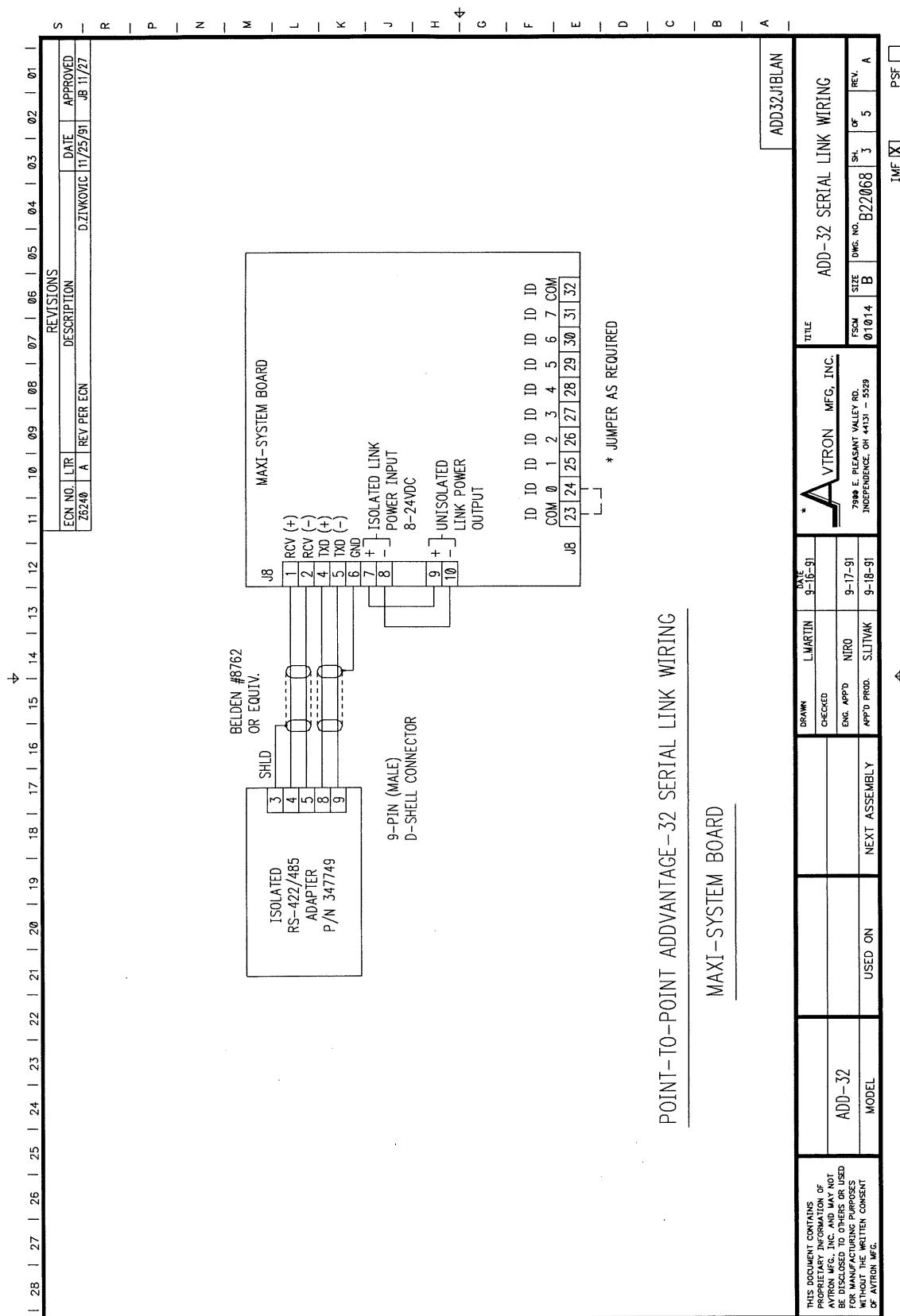


Figure 10-1. ADD-32 Serial Link Wiring (Sheet 2 of 3)

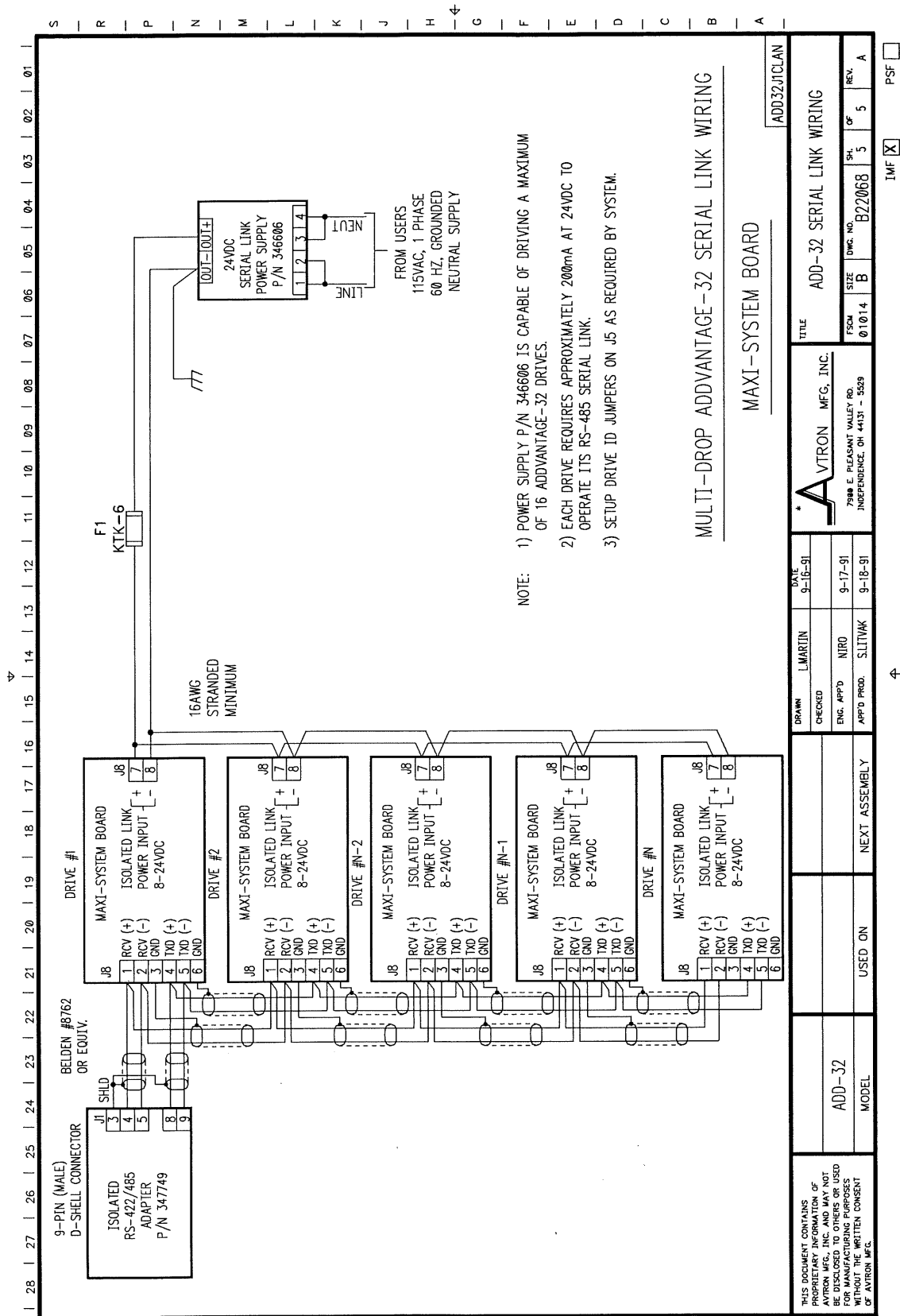
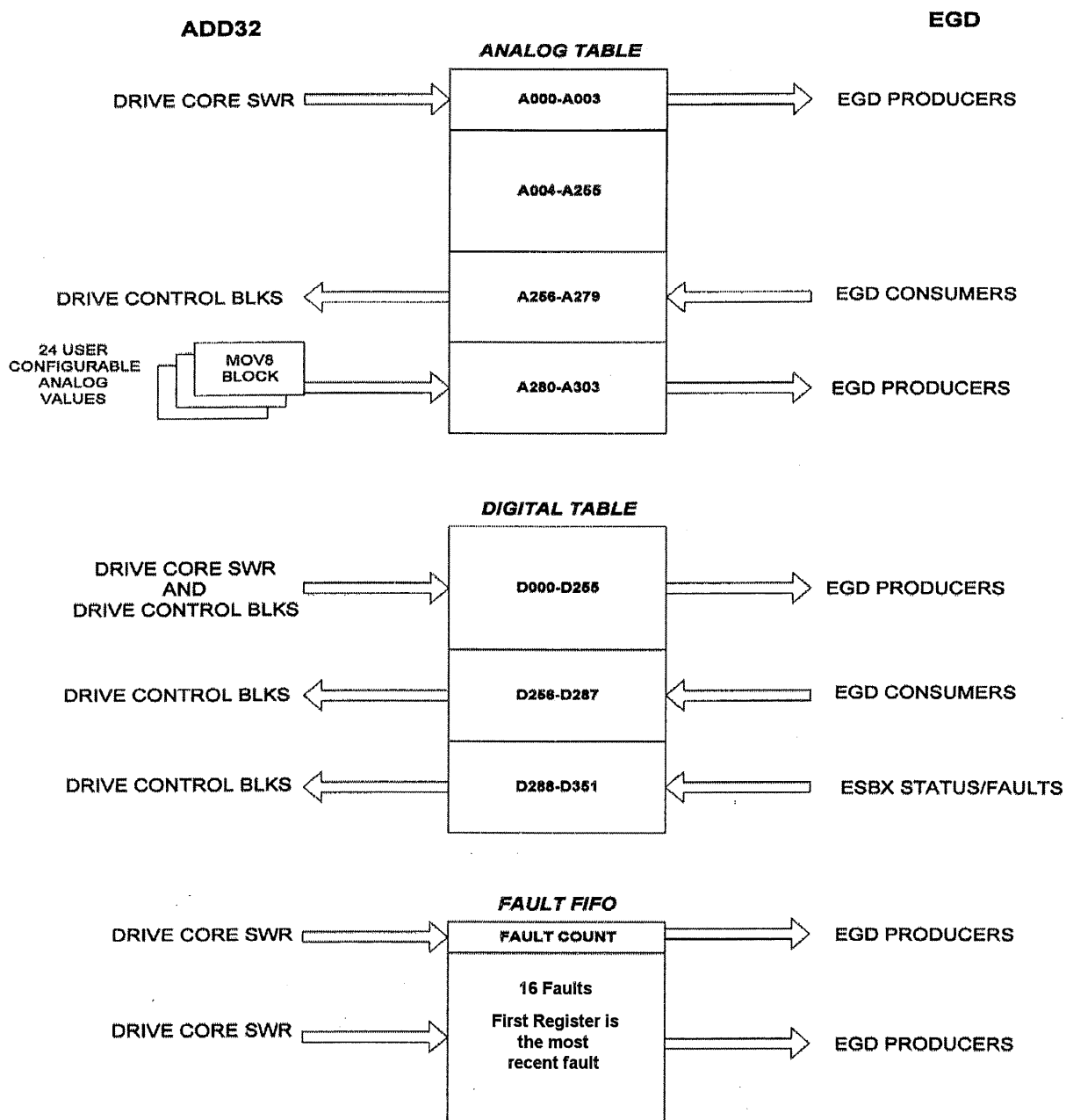


Figure 10-1. ADD-32 Serial Link Wiring (Sheet 3 of 3)

## ADD32-EGD INTERFACE



ADD32H1LAN

Figure F-1. ADDvantage-32 Digital Drive to EGD Interface Diagram

TABLE 10-1. RS-232C PIN ASSIGNMENTS

The following table is a complete list of RS232 pin assignments for DB25 and DB9 connectors.  
(\* REPRESENTS MOST USED PINS)

DB25	DB9	FUNCTION	DEFINITION	DIRECTION
1 *		Ground	Chassis Ground	NA
2 *	3	Data Xfer	Transmit Data	from DTE to DCE
3 *	2	Data Xfer	Receive Data	from DCE to DTE
4 *	7	Control	Request to send (RTS)	from DTE to DCE
5 *	8	Control	Clear to send (CTS)	from DCE to DTE
6 *	6	Control	Data set ready (DSR)	from DCE to DTE
7 *	5	Ground	Signal ground	NA
8 *	1	Control	Data carrier detect (DCD)	from DCE to DTE
9		Test	Data set testing	NA
10		Test	Data set testing	NA
11		-	Not assigned	NA
12		Control	Secondary DCD	from DCE to DTE
13		Control	Secondary CTS	from DCE to DTE
14		Control	Secondary transmit data	from DTE to DCE
15		Timing	Transmit on signal element timing	from DCE to DTE
16		Control	Secondary receive data	from DCE to DTE
17		Timing	Received signal element timing	from DCE to DTE
18		-	Not assigned	NA
19		Control	Secondary RTS	from DTE to DCE
20 *	4	Control	Data terminal ready (DTR)	from DTE to DCE
21		Control	Signal quality detector	from DCE to DTE
22 *	9	Control	Ring indicator (RI) modem	from DCE to DTE
23		Timing	Data signal rate selector	either
24		Timing	Transmission signal element timing	from DTE to DCE
25		-	Not assigned	NA



TABLE 10-2. PROBLEMS WITH THE SERIAL LINK

SYMPTOM	PROBLEM/SOLUTION
Xmit light on 485 card does not blink 6 times while ADDapt attempts to connect.	Computer/485 card configuration is not compatible. To fix, see 485 card instructions and computer setup instructions. The 485 card must have its CTS DISABLED. An internal 485 card must have its defined COM port (usually a jumper on the card) DISABLED in the computer's setup. For an external 485 card, the computer must have its serial port ENABLED. The proper COM port must be defined in CONFIG also.
RCV LED on system board does not flash 6 times while ADDapt tries to connect.	Check 485 card xmit light first. If LED is on all the time, check receive wires to J8, pins 1, 2. If that does not solve the problem, check for power (8 - 28VDC) at ISO PWR IN. Check for 5VDC on pin 8 of U10. If 5V not present, link circuit is damaged; replace board.
RCV LED on system board flashes 6 times but does not connect.	<p>Baud rates are incompatible: Change LINK BAUD in drive and reset. If that does not solve the problem, when entering ADDapt, type ADDAPT -bxxxx, where xxxx is either 4800 or 9600. This will override the default computer baud rate. If that does not solve the problem, change default baud rate in CONFIG.SYS by adding BAUD=xxxx and reboot.</p> <p>Serial link addresses are incompatible. Change in CONFIG; if that does not solve the problem, change jumpers on system board.</p> <p>Software part no. and version no. of flash prom do not match CONFIG.</p> <p>If the above is OK and the receive LED on 485 card flashes, replace the 485 card or replace the Bridge Interface board.</p>
ADDapt will not link reliably and/or loses the link spontaneously.	If all configuration is good, then either EMI noise or hardware is the problem. Check for loose wiring or change out BI board, 485 card or CPU. Cable should be two twisted, shielded pairs. Shields should be grounded at transmit end only. Do not run wiring in high voltage raceway or parallel to any high voltage or AC wiring.